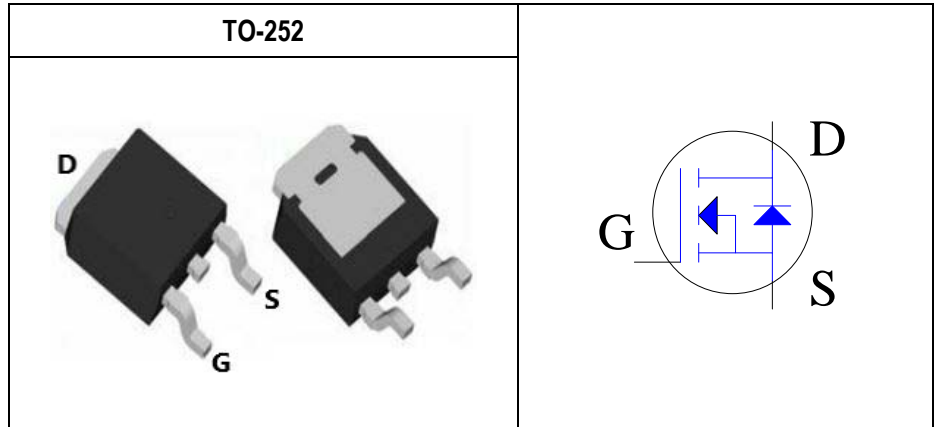


Parameter	Value	Unit
V_{DSS}	100	V
$R_{DS(ON) max. V_{GS}=10V}$	9.1	m Ω
I_D	91	A
$V_{GS(TH) Typ.}$	1.6	V
$C_{iss} Typ.$	2401	pF
$Q_{g10V} Typ.$	48.9	nC
E_{AS}	14.4	mJ



Features	Application
<ul style="list-style-type: none"> Low On-Resistance $R_{DS(on)}$ Low Input Capacitance Low Gate Charge Fully Characterized Capacitance and Avalanche Pb-free lead plating; RoHS compliant 	<ul style="list-style-type: none"> Quick Charger DC to DC Converter Switch Mode Power Supply With Logic Level Driving Application Synchronous Rectifier for Power Delivery

Ordering Information

Ordering Code	RoHS Status	Package	Package Code	Packing	Quantity
DG100N03D	Halogen-Free	TO-252	D	Tape & Reel	2,500

Absolute Maximum Ratings ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous ^{Note 1}	I_D	$T_C=25^\circ\text{C}$	91
		$T_C=100^\circ\text{C}$	58
Drain Current-Continuous ^{Note 2}	I_D	$T_A=25^\circ\text{C}$	13.7
		$T_A=70^\circ\text{C}$	10.9
Drain Current-Pulsed ^{Note 3}	I_{DM}	140	A
Avalanche Current	I_{AR}	17	A
Single Pulse Avalanche Energy ^{Note 4}	E_{AS}	14.4	mJ
Maximum Power Dissipation	P_D	$T_C=25^\circ\text{C}$	140
		$T_C=100^\circ\text{C}$	56
		$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal resistance, Junction-Case ^{Note 5}	$R_{\theta JC}$	Steady State	-	-	0.89	$^\circ\text{C/W}$
Thermal resistance, Junction-Ambient ^{Note 5}	$R_{\theta JA}$	Steady State	-	-	40	$^\circ\text{C/W}$

Notes:

- Limited by silicon chip capability and $R_{\theta JC}$ junction-to-case thermal resistance.
- The maximum current rating is limited by package and $R_{\theta JA}$ junction-to-ambient thermal resistance.
- Must be ensure junction temperature does not exceed 150-degree C. (Pulse Width $\leq 100\mu\text{s}$, Duty $\leq 2\%$)
- Limited by T_{Jmax} , starting $T_J=25^\circ\text{C}$, $L=0.1\text{mH}$, $R_g=25\Omega$, $I_D=17\text{A}$, $V_{GS}=10\text{V}$.
- The value of thermal resistance is measured with the single device put on cooling plate under a still air environment temperature is 25 degree C based on JEDEC standard JESD51-14 and JESD51-2a. Thermal resistance obtained depends on the user's specific board design and given application.

Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _{DS} =-250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =80V, V _{GS} =0V	-	-	1	μA
		V _{DS} =80V, V _{GS} =0V, T _J =125°C	-	-	10	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA

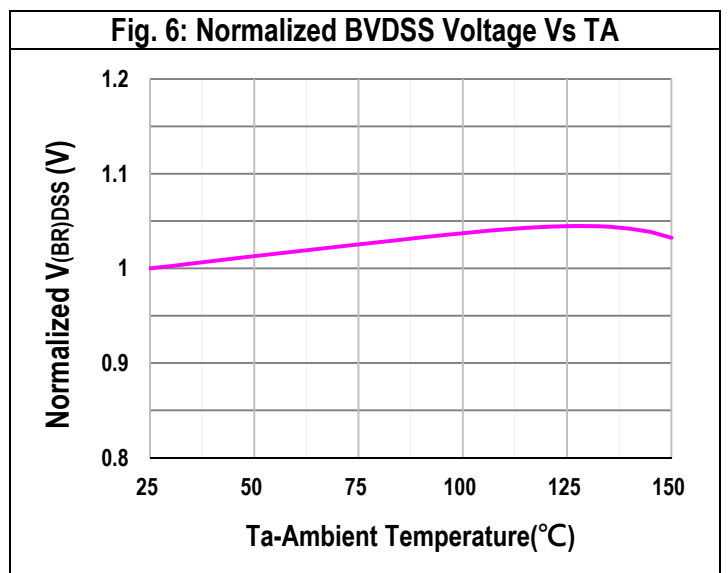
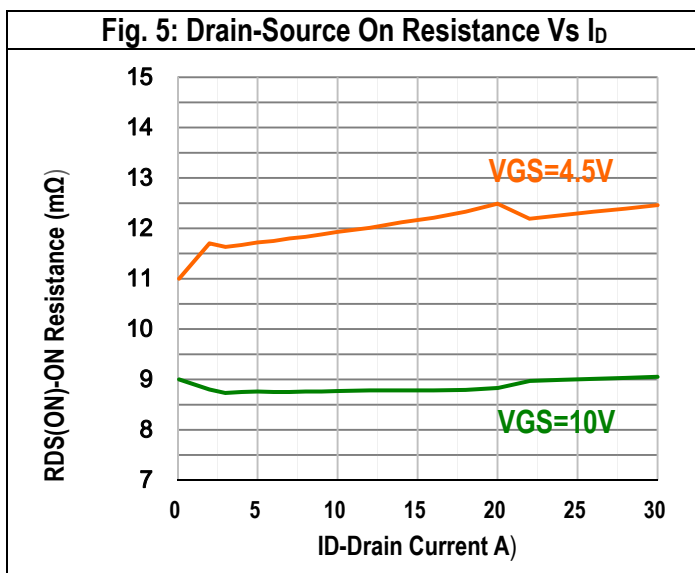
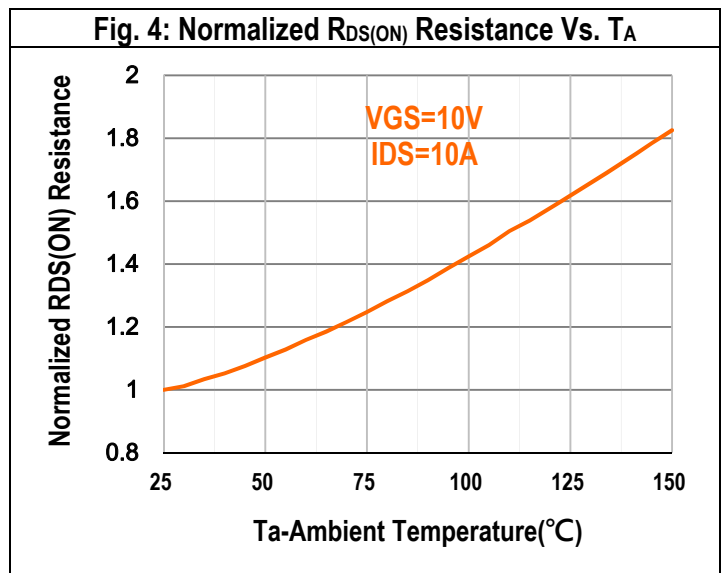
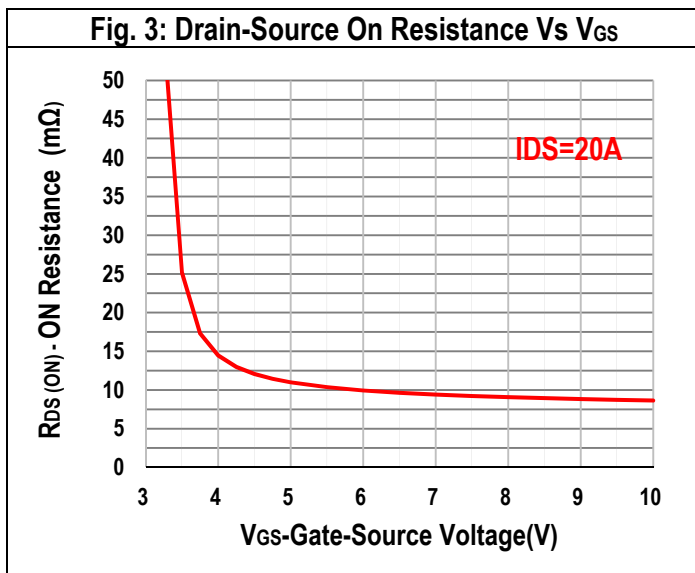
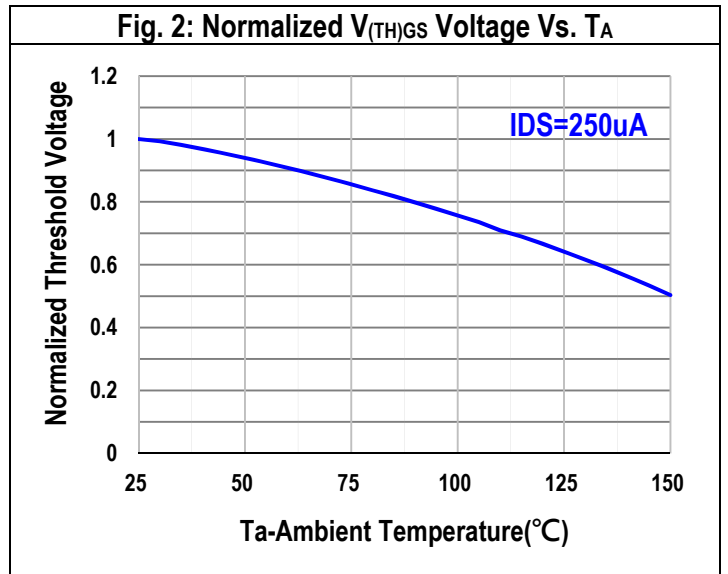
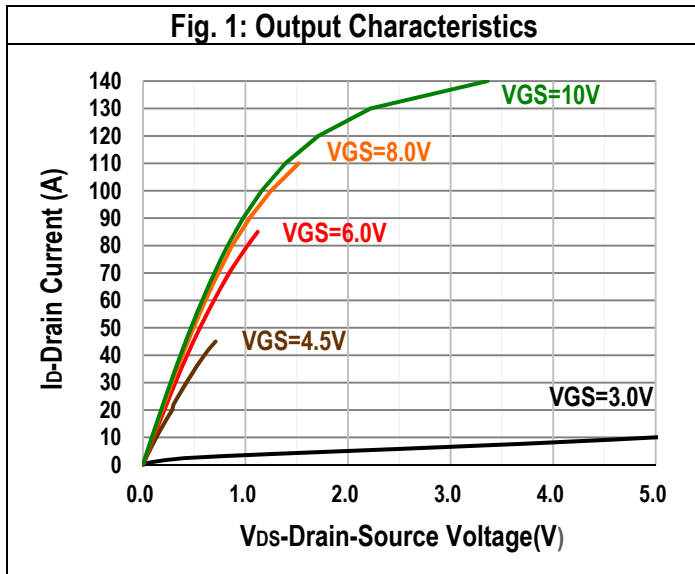
STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _{DS} =250μA	1.3	1.6	1.9	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _{DS} =20A	-	8.4	9.1	mΩ
		V _{GS} =4.5V, I _{DS} =10A	-	11.5	13.2	mΩ
Gate Resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	0.66	-	Ω
Forward Transconductance	g _{fs}	V _{DS} =5V, I _{DS} =20A	-	25	-	S

DYNAMIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C _{iss}	V _{DD} =100V, V _{DS} =50V, V _{GS} =0V, f=1MHz	-	2401	-	pF
Output Capacitance	C _{oss}	V _{DD} =100V, V _{DS} =50V, V _{GS} =0V, f=1MHz	-	269	-	pF
Reverse Transfer Capacitance	C _{rss}	V _{DD} =100V, V _{DS} =50V, V _{GS} =0V, f=1MHz	-	7.2	-	pF
Turn-On Delay Time	T _{d(on)}	V _{DS} =50V, V _{GS} =10V, I _{DS} =20A, R _{GEN} =3.0Ω	-	10.6	-	nS
Rise Time	T _r	V _{DS} =50V, V _{GS} =10V, I _{DS} =20A, R _{GEN} =3.0Ω	-	31.1	-	nS
Turn-Off Delay Time	T _{d(off)}	V _{DS} =50V, V _{GS} =10V, I _{DS} =20A, R _{GEN} =3.0Ω	-	37.1	-	nS
Fall Time	T _f	V _{DS} =50V, V _{GS} =10V, I _{DS} =20A, R _{GEN} =3.0Ω	-	55.1	-	nS

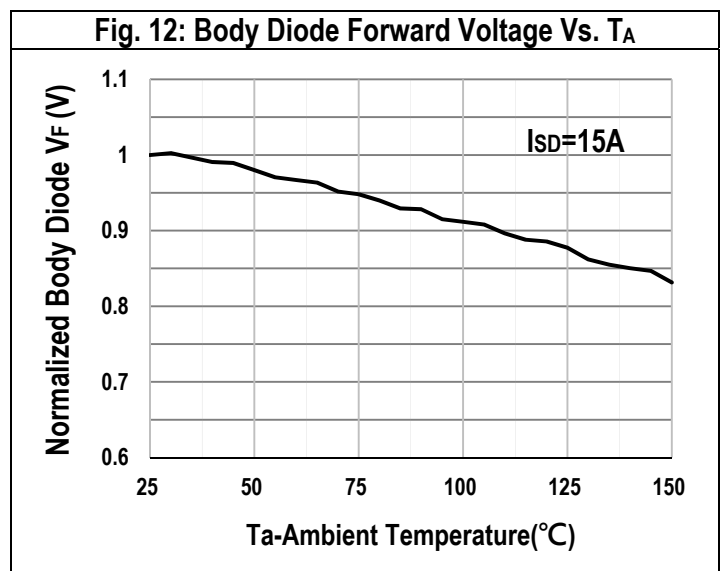
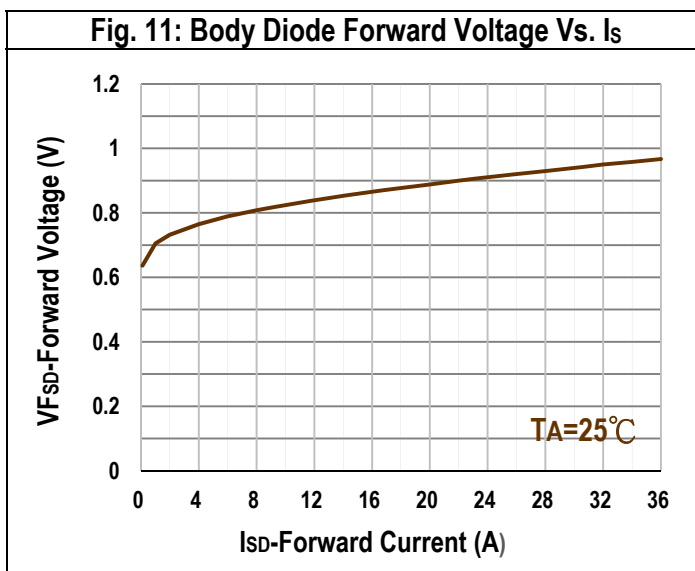
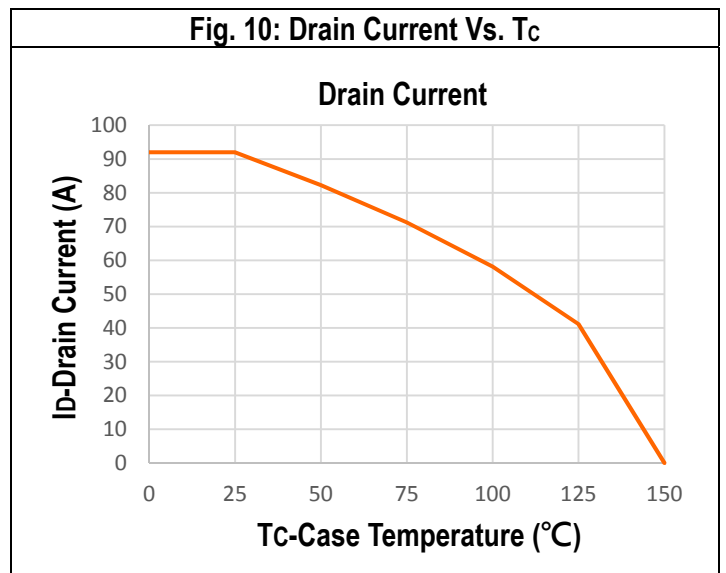
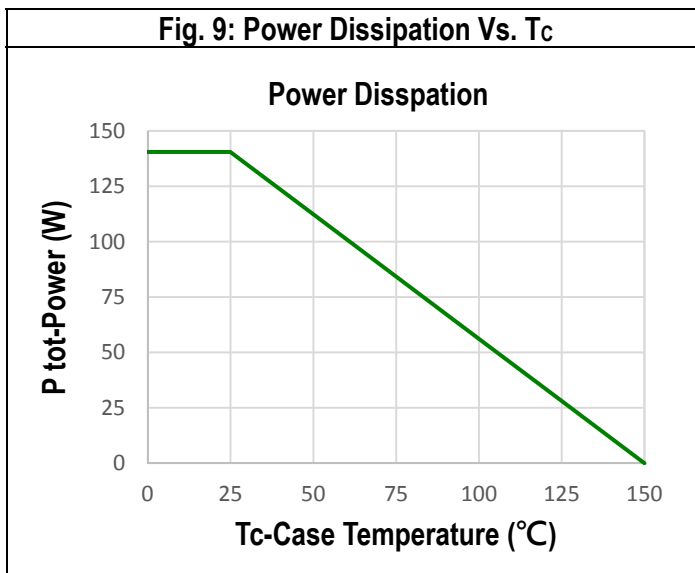
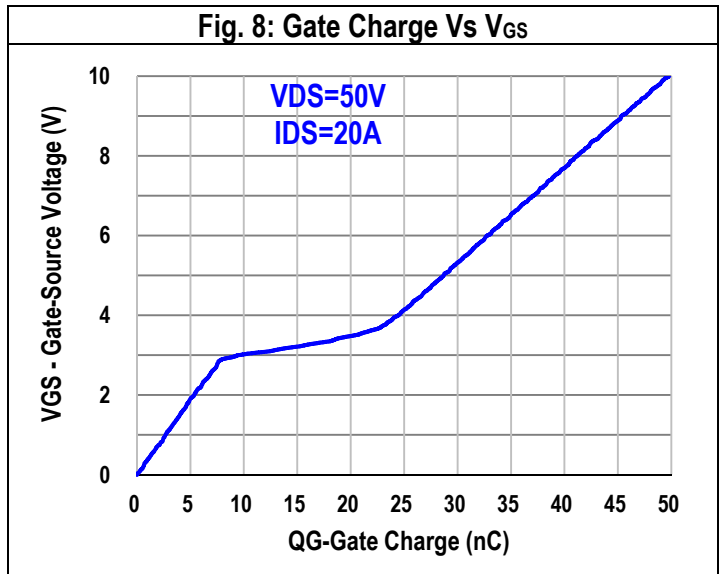
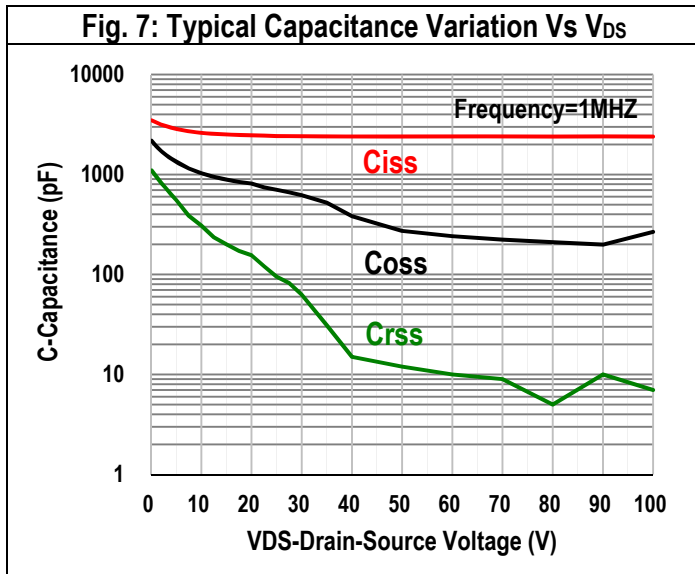
GATE CHARGE CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate to Source Gate Charge	Q _{gs}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	8.3	-	nC
Gate charge at threshold	Q _{g(th)}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	4	-	nC
Gate to Drain Charge	Q _{gd}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	14.6	-	nC
Switching charge	Q _{sw}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	19	-	nC
Gate charge total	Q _{g 10V}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	48.9	-	nC
Gate plateau voltage	V _{plateau}	V _{DD} =50V, I _D =20A, V _{GS} =0 to 10V	-	3.3	-	V
Gate charge total, sync. FET (Q _g - Q _{gd})	Q _{g(sync)}	V _{DS} =0.1V, V _{GS} =0 to 10V	-	44.9	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Body Diode continuous forward current	I _s	T _C =25°C	-	-	36	A
Body Diode pulse current	I _{SM}	T _C =25°C	-	-	140	A
Body Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _s =20A	-	0.87	1.0	V
Body Diode Reverse Recovery Time	t _{rr}	V _{DD} =50V, I _F =20A, di/dt=200A/μs	-	29.7	-	nS
Body Diode Reverse Recovery Charge	Q _{rr}	V _{DD} =50V, I _F =20A, di/dt=200A/μs	-	53.5	-	nC
Body Diode Reverse Recovery Current	I _{rm}	V _{DD} =50V, I _F =20A, di/dt=200A/μs	-	3.2	-	A

Typical Operating Characteristics



Typical Operating Characteristics



4. Typical Operating Characteristics

Fig. 13: Safe Operation Area

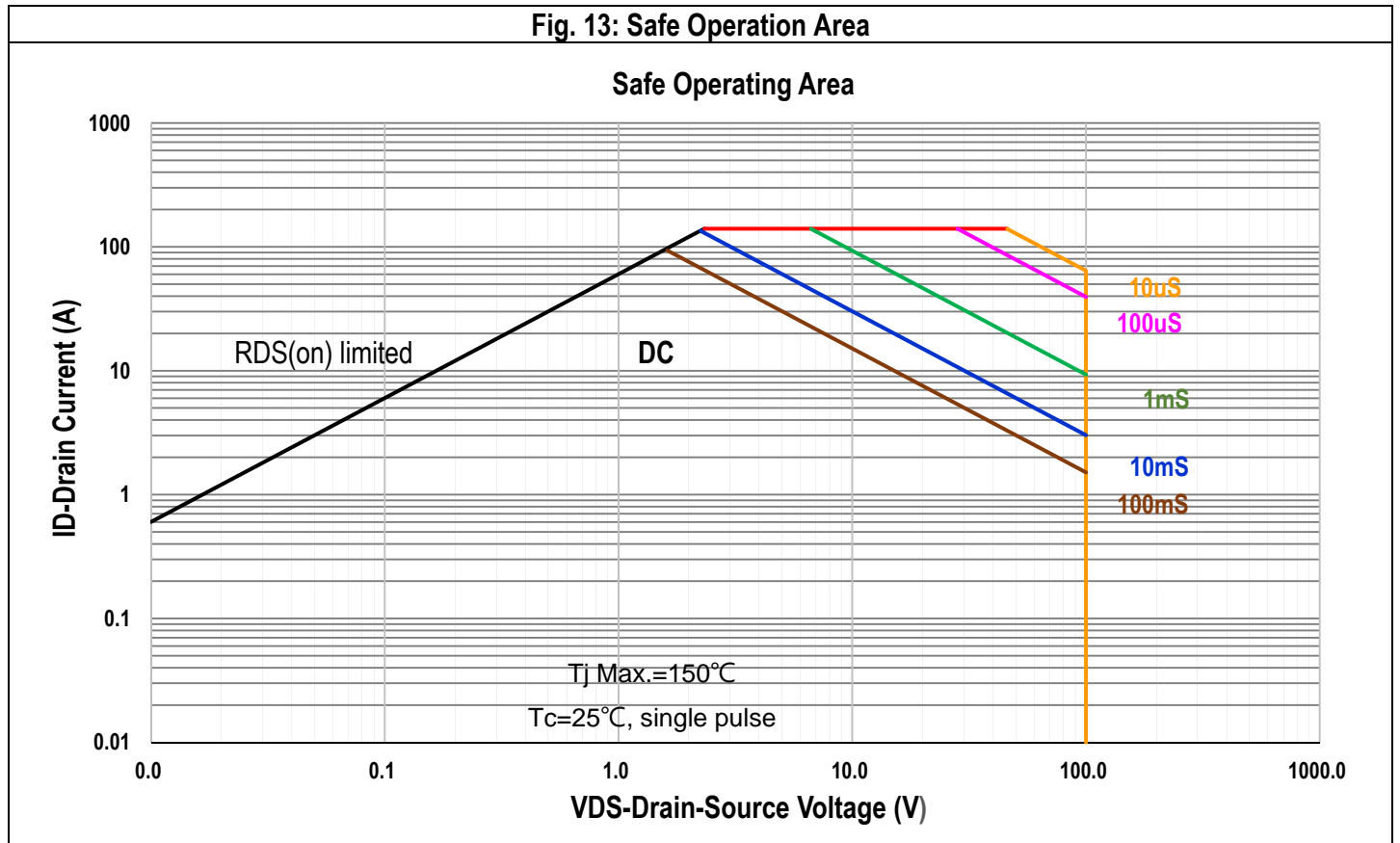
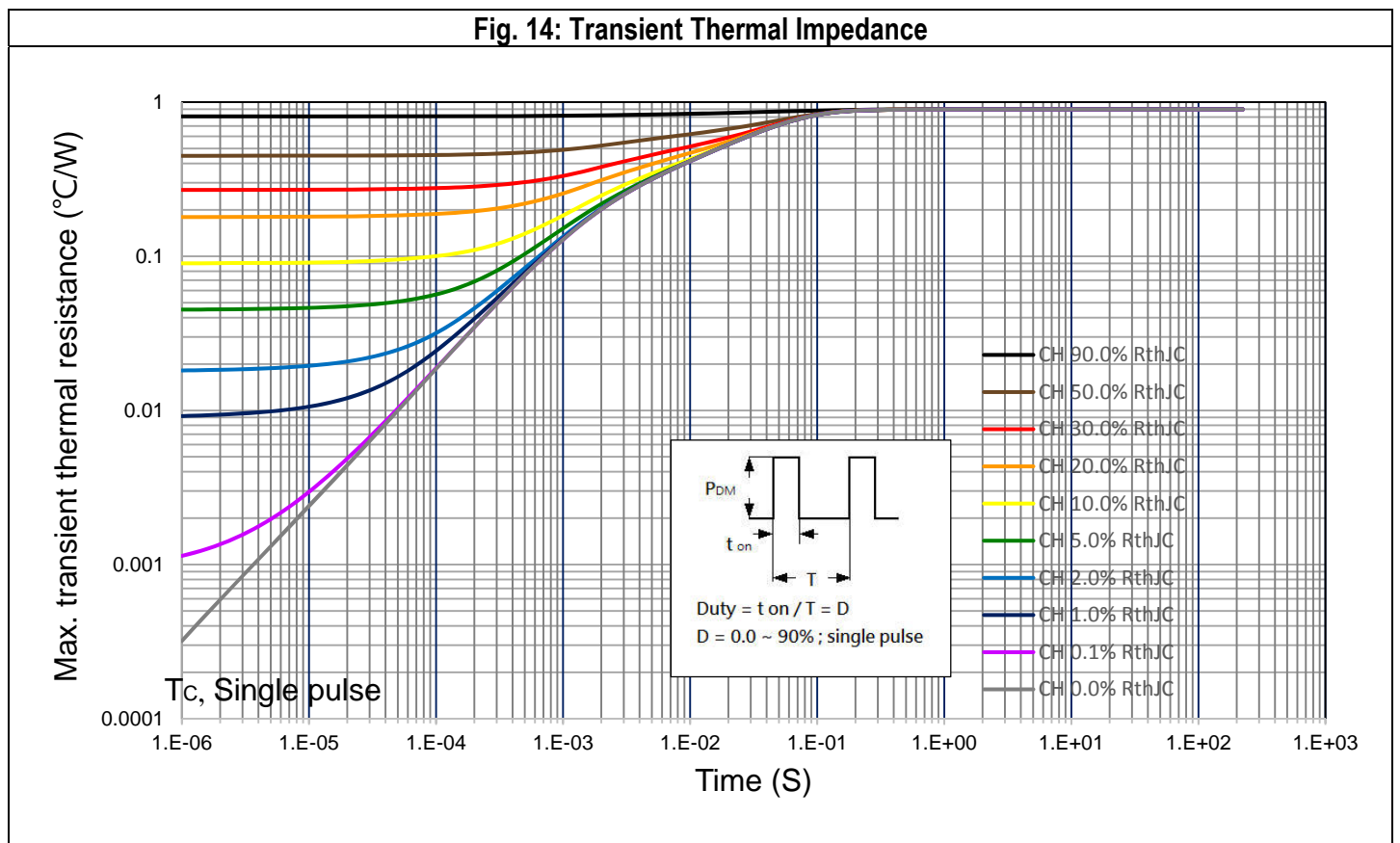
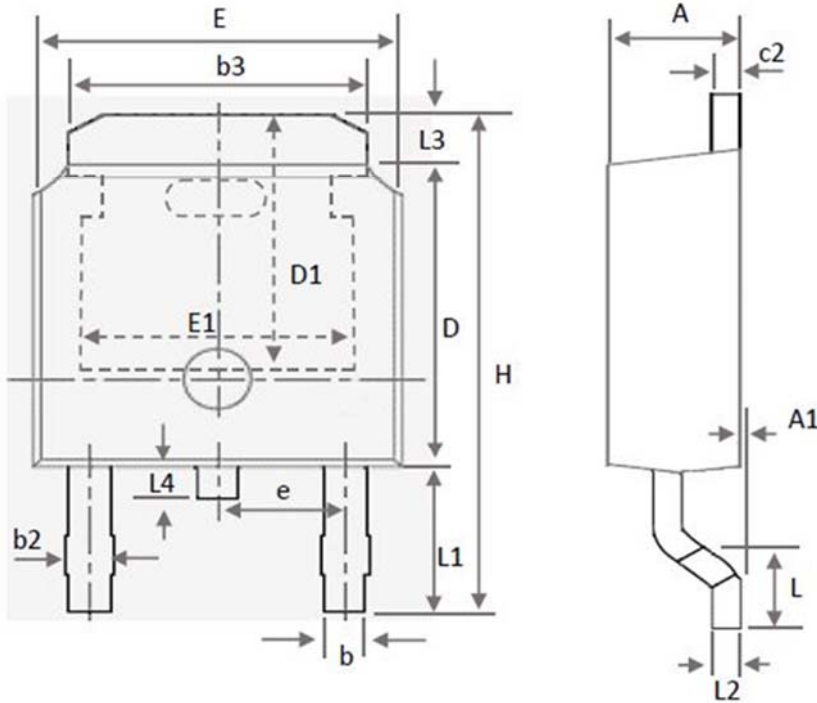


Fig. 14: Transient Thermal Impedance

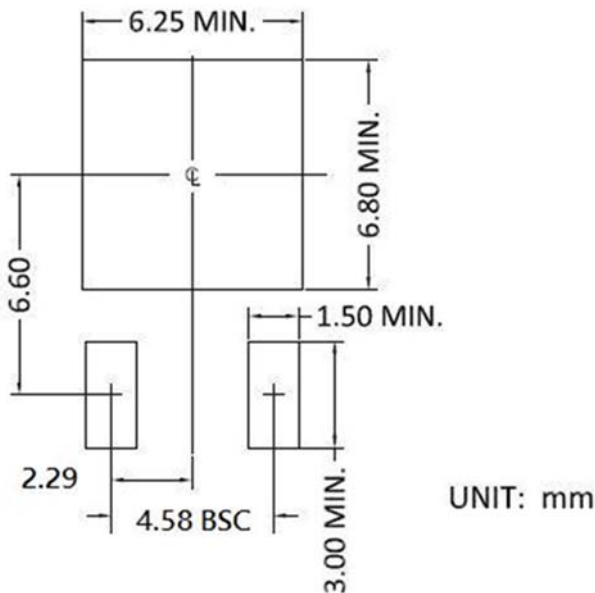


Package of Dimension



Symbol	Min	Nor	Max
E	6.35	6.54	6.731
L	1.40	1.59	1.78
L1	2.743 Ref.		
L2	0.508 BSC		
L3	0.89	1.08	1.27
L4	0.60	0.81	1.01
D	5.97	6.10	6.223
H	9.40	9.91	10.41
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	4.95	5.21	5.46
e	2.286 BSC		
A	2.18	2.29	2.39
A1	0.00	0.07	0.13
c2	0.46	0.68	0.89
D1	5.21	-	-
E1	4.32	-	-

Land Pattern (Footprint)



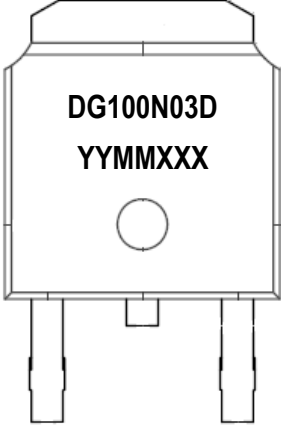
Note 1: Land pattern (Footprint) design is for reference only.

Note 2: Package body sizes exclude mold flash and burrs.

Note 3: Dimension is measured in gauge plane.

Note 4: Tolerance 0.1mm unless otherwise specified.

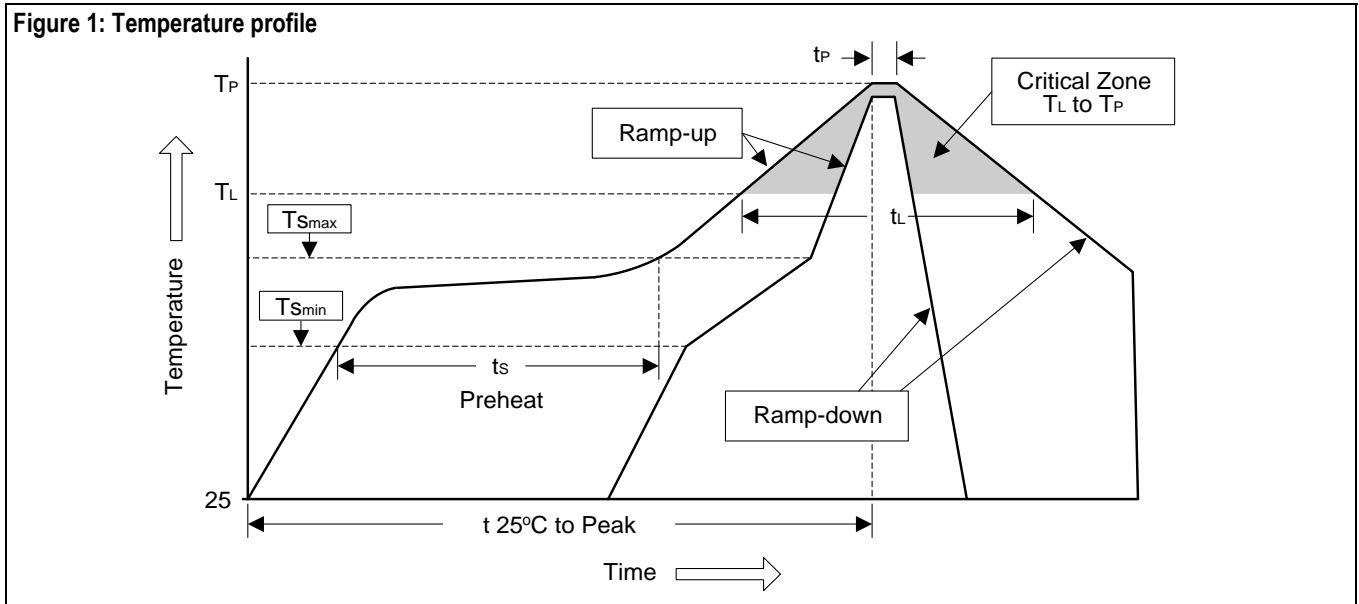
Marking Information

TO-252 (D)	Marking Rule
<p>Laser Marking</p>  <p>The diagram shows a TO-252 (D) MOSFET package. The top surface is marked with the device identifier 'DG100N03D' and the date code 'YYMMXXX'. The package has three leads extending from the bottom.</p>	<p><u>Line 1</u> : Device DG100N03D</p> <p><u>Line 2</u> : Date Code YYMMXXX</p> <p>YY : Year Code MM : Month Code XXX : Serial Number</p>

Appendix-A

Soldering Methods for Silicongear's Products (Just for SMD type of device)

- Storage environment: Temperature=10°C to 35°C Humidity=65%±15%
- Reflow soldering of surface-mount devices



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T _L to T _P)	<3°C/sec	<3°C/sec
Preheat		
- Temperature Min (T _{smin})	100°C	150°C
- Temperature Max (T _{smax})	150°C	200°C
- Time (min to max) (ts)	60 to 120 sec	60 to 180 sec
T _{smax} to T _L		
- Ramp-up Rate	<3°C/sec	<3°C/sec
Time maintained above:		
- Temperature (T _L)	183°C	217°C
- Time (t _L)	60 to 150 sec	60 to 150 sec
Peak Temperature (T _P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t _P)	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

Appendix-B**Important Notice****© Silicongear Corporation**

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