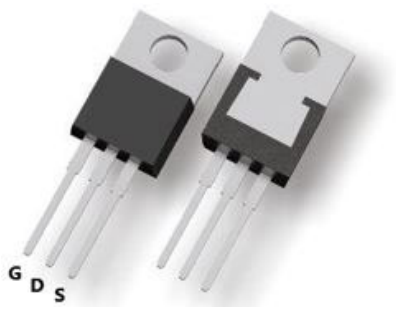
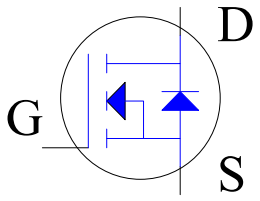
DG100N03PB

***DG-FET*™ 100V N-Channel Power MOSFET**

Parameter	Value	Unit
V_{DSS}	100	V
$R_{DS(ON)\ max.}$ V_{GS}=10V	10.0	mΩ
$R_{DS(ON)\ max.}$ V_{GS}=4.5V	13.0	mΩ
I_D	91.4	A
Q_{g10v}	38.6	nC
Q_{gd}	10.8	nC
Q_{sw}	14.6	nC

TO-220AB-D





Features

- Low On-Resistance $R_{DS\ (on)}$
- Low Input Capacitance
- Low Gate Charge
- Fully Characterized Capacitance and Avalanche
- Pb-free lead plating; RoHS compliant

Application

- Quick Charger
- DC to DC Converter
- Switch Mode Power Supply
- With Logic Level Driving Application
- Synchronous Rectifier for Power Delivery

Ordering Information

Ordering Code	RoHS Status	Package	Package Code	Packing	Quantity
DG100N03PB	Halogen-Free	TO-220AB-D	PB	Tube	50

Absolute Maximum Ratings (T_J=25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous Note 1	T_C=25°C	I_D	91.4	A
	T_C=100°C		57.8	A
Drain Current-Continuous Note 2	T_A=25°C	I_D	13.1	A
	T_A=70°C		10.5	A
Drain Current-Pulsed Note 3	T_C=25°C	I_{DM}	140	A
Avalanche Current		I_{AR}	26.2	A
Single Pulse Avalanche Energy Note 4		E_{AS}	34.4	mJ
Maximum Power Dissipation	T_C=25°C	P_D	161.9	W
	T_C=100°C		64.8	W
	T_A=25°C		3.3	W
	T_A=70°C		2.1	W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal resistance, Junction-Case Note 5	$R_{\theta JC}$	Steady State	-	-	0.8	°C/W
Thermal resistance, Junction-Ambient Note 5	$R_{\theta JA}$	Steady State	-	-	34.1	°C/W

Notes:

1. Limited by silicon chip capability and $R_{\theta JC}$ junction-to-case thermal resistance.
2. The maximum current rating is limited by package and $R_{\theta JA}$ junction-to-ambient thermal resistance.
3. Must be ensure junction temperature does not exceed 150-degree C. (Pulse Width ≦ 100uS, Duty ≦ 2%)
4. Limited by T_{Jmax}, starting T_J=25°C, L=0.1mH, R_g=25Ω, I_D=26.2A, V_{GS}=10V.
5. The value of thermal resistance is measured with the single device put on cooling plate under a still air environment temperature is 25 degree C based on JEDEC standard JESD51-14 and JESD51-2a. Thermal resistance obtained depends on the user's specific board design and given application.

Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_{DS}=250µA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	µA
		V_{DS}=100V, V_{GS}=0V, T_J=125°C	-	-	100	µA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_{DS}=250µA	1.2	1.6	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_{DS}=20A	-	8.3	10.0	mΩ
		V_{GS}=4.5V, I_{DS}=10A		10.8	13.0	mΩ
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	0.6	-	Ω
Forward Transconductance	g_{fs}	V_{DS}=5V, I_{DS}=5A	-	18.0	-	S

DYNAMIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Capacitance	C_{iss}	V_{DD}=100V, V_{DS}=50V, V_{GS}=0V, f=1MHz	-	1741.8	-	pF
Output Capacitance	C_{oss}	V_{DD}=100V, V_{DS}=50V, V_{GS}=0V, f=1MHz	-	273.3	-	pF
Reverse Transfer Capacitance	C_{rss}	V_{DD}=100V, V_{DS}=50V, V_{GS}=0V, f=1MHz	-	13.5	-	pF
Turn-On Delay Time	$T_{d(on)}$	V_{DS}=50V, V_{GS}=10V, I_{DS}=20A, R_{GEN}=2.4Ω	-	9.7	-	nS
Rise Time	T_r	V_{DS}=50V, V_{GS}=10V, I_{DS}=20A, R_{GEN}=2.4Ω	-	33	-	nS
Turn-Off Delay Time	$T_{d(off)}$	V_{DS}=50V, V_{GS}=10V, I_{DS}=20A, R_{GEN}=2.4Ω	-	28.1	-	nS
Fall Time	T_f	V_{DS}=50V, V_{GS}=10V, I_{DS}=20A, R_{GEN}=2.4Ω	-	60.7	-	nS

GATE CHARGE CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate to Source Gate Charge	Q_{gs}	V_{DD}=50V, I_D=20A, V_{GS}=0 to 10V	-	6.8	-	nC
Gate charge at threshold	$Q_{g(th)}$	V_{DD}=50V, I_D=20A, V_{GS}=0 to 10V	-	3	-	nC
Gate to Drain Charge	Q_{gd}	V_{DD}=50V, I_D=20A, V_{GS}=0 to 10V	-	10.8	-	nC
Switching charge	Q_{SW}	V_{DD}=50V, I_D=20A, V_{GS}=0 to 10V	-	14.6	-	nC
Gate charge total	$Q_{g\ 10V}$	V_{DD}=50V, I_D=20A, V_{GS}=0 to 10V	-	38.6	-	nC
	$Q_{g\ 4.5V}$	V_{DD}=50V, I_D=20A, V_{GS}=0 to 10V	-	20.2	-	nC
Gate plateau voltage	$V_{plateau}$	V_{DD}=50V, I_D=20A, V_{GS}=0 to 10V	-	3.4	-	V
Gate charge total, sync. FET (Q_g- Q_{gd})	$Q_{g(sync)}$	V_{DS}=0.1V, V_{GS}=0 to 10V	-	27.8	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Body Diode continuous forward current	I_S	T_C=25°C	-		91.4	A
Body Diode pulse current	I_{SM}	T_C=25°C	-	-	140	A
Body Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=20A	-	0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	V_{DD}=50V, I_F=20A, di/dt=100A/µs	-	40.2	-	nS
		V_{DD}=50V, I_F=20A, di/dt=200A/µs		38.3		nS
Body Diode Reverse Recovery Charge	Q_{rr}	V_{DD}=50V, I_F=20A, di/dt=100A/µs	-	31.8	-	nC
		V_{DD}=50V, I_F=20A, di/dt=200A/µs		75.7		nC

Typical Operating Characteristics

Fig. 1: Output Characteristics

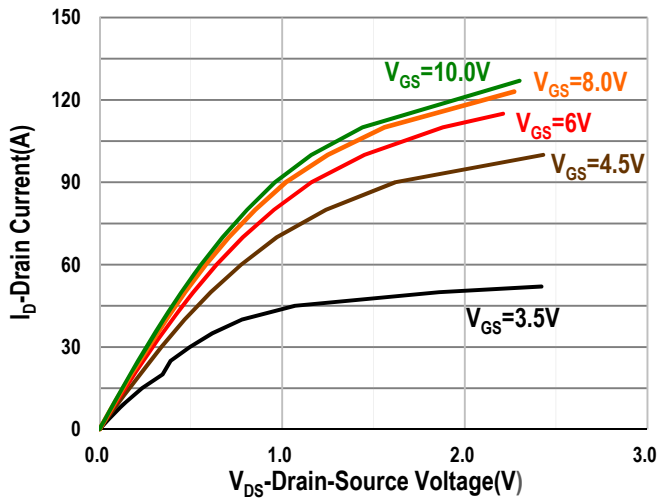


Fig. 2: Normalized $V_{(TH)GS}$ Voltage Vs. T_A

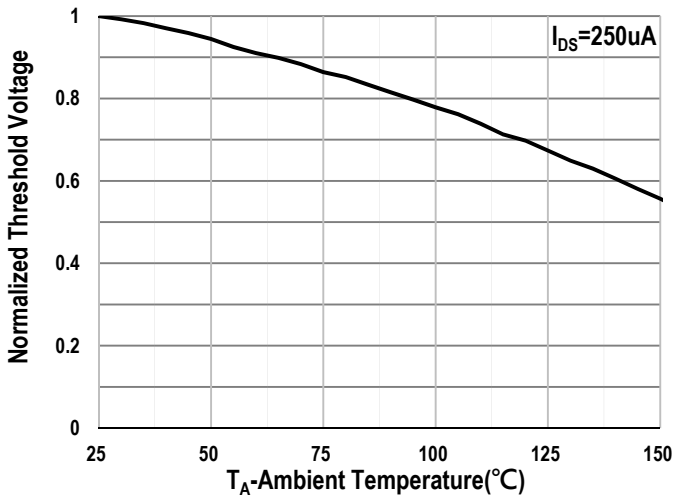


Fig. 3: Drain-Source On Resistance Vs V_{GS}

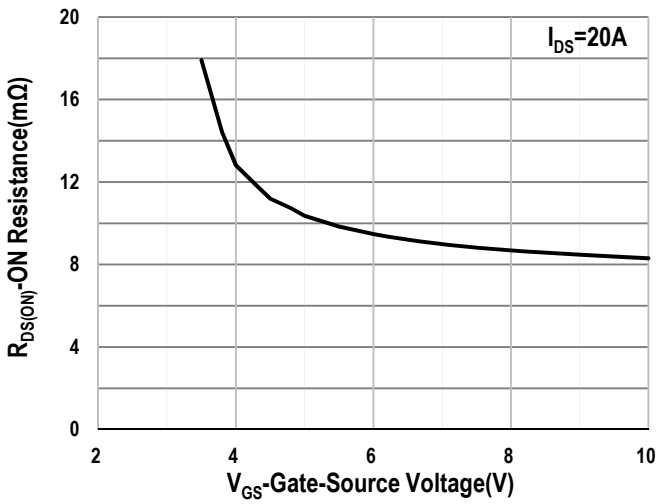


Fig. 4: Normalized $R_{DS(ON)}$ Resistance Vs. T_A

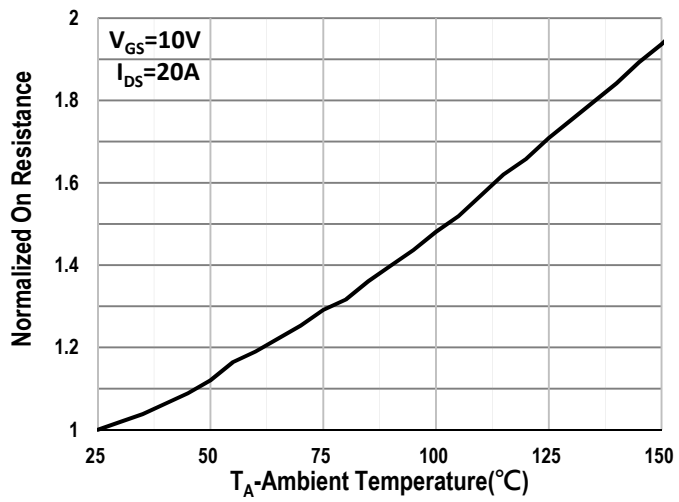


Fig. 5: Drain-Source On Resistance Vs I_D

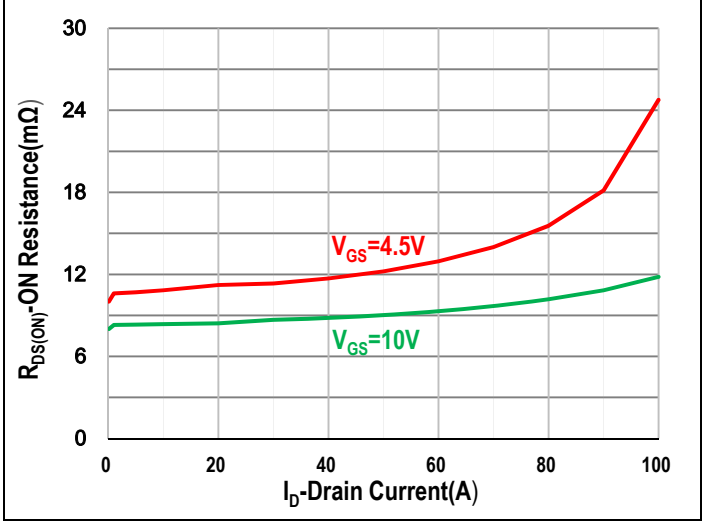
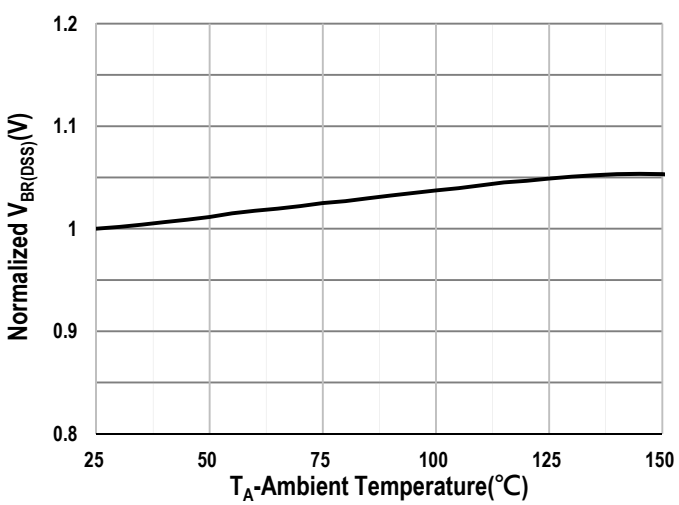


Fig. 6: Normalized BV_{DSS} Voltage Vs T_A



Typical Operating Characteristics

Fig. 7: Typical Capacitance Variation Vs V_{DS}

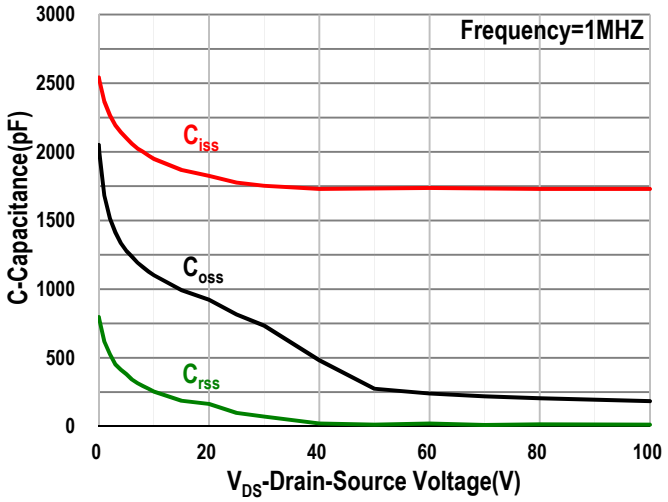


Fig. 8: Gate Charge Vs V_{GS}

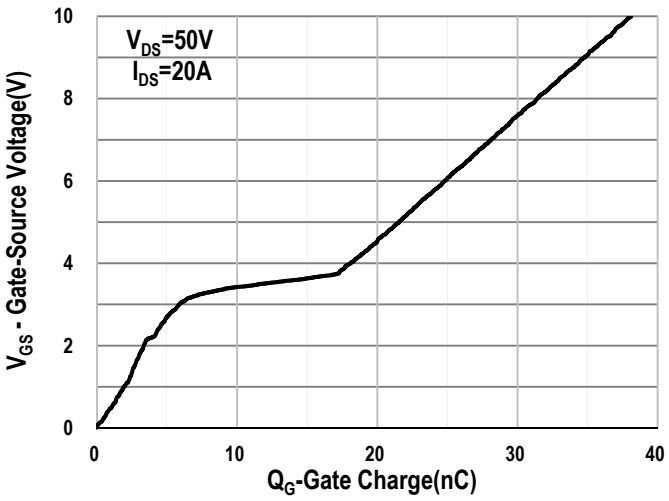


Fig. 9: Power Dissipation Vs. T_C

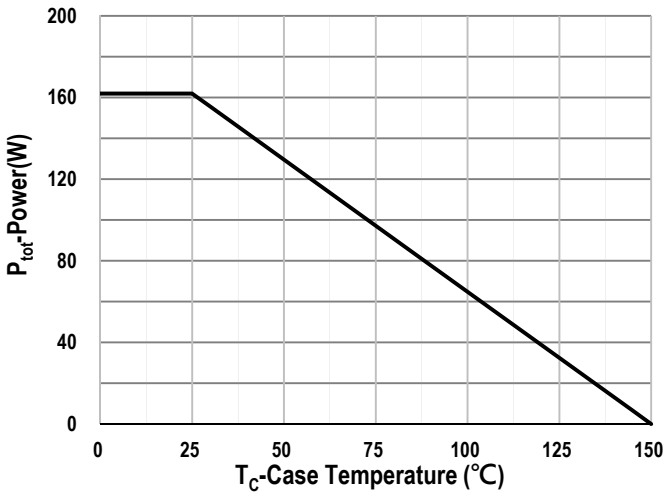


Fig. 10: Drain Current Vs. T_C

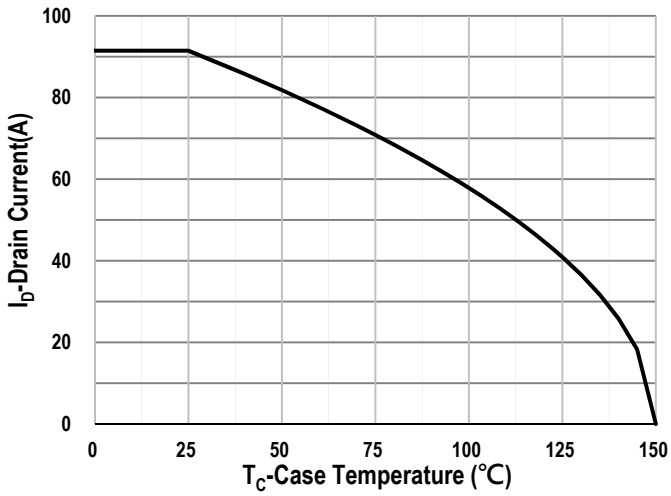


Fig. 11: Body Diode Forward Voltage Vs. I_S

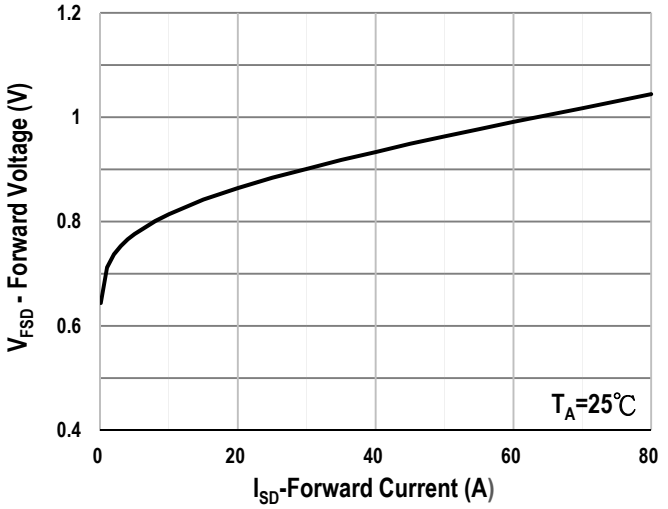
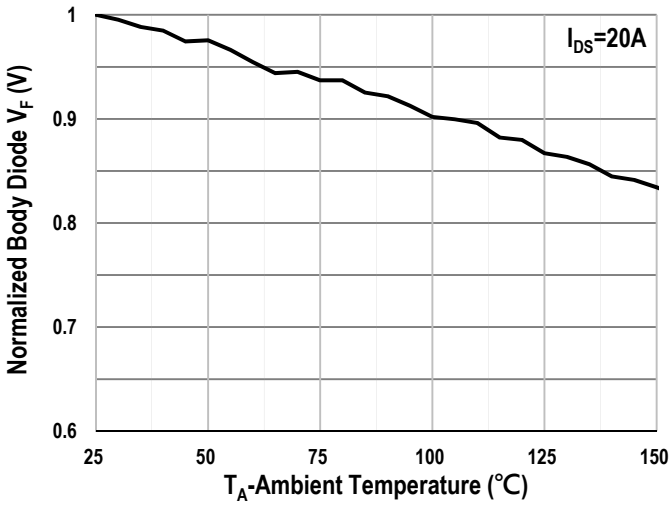


Fig. 12: Body Diode Forward Voltage Vs. T_A



Typical Operating Characteristics

Fig. 13: Safe Operation Area

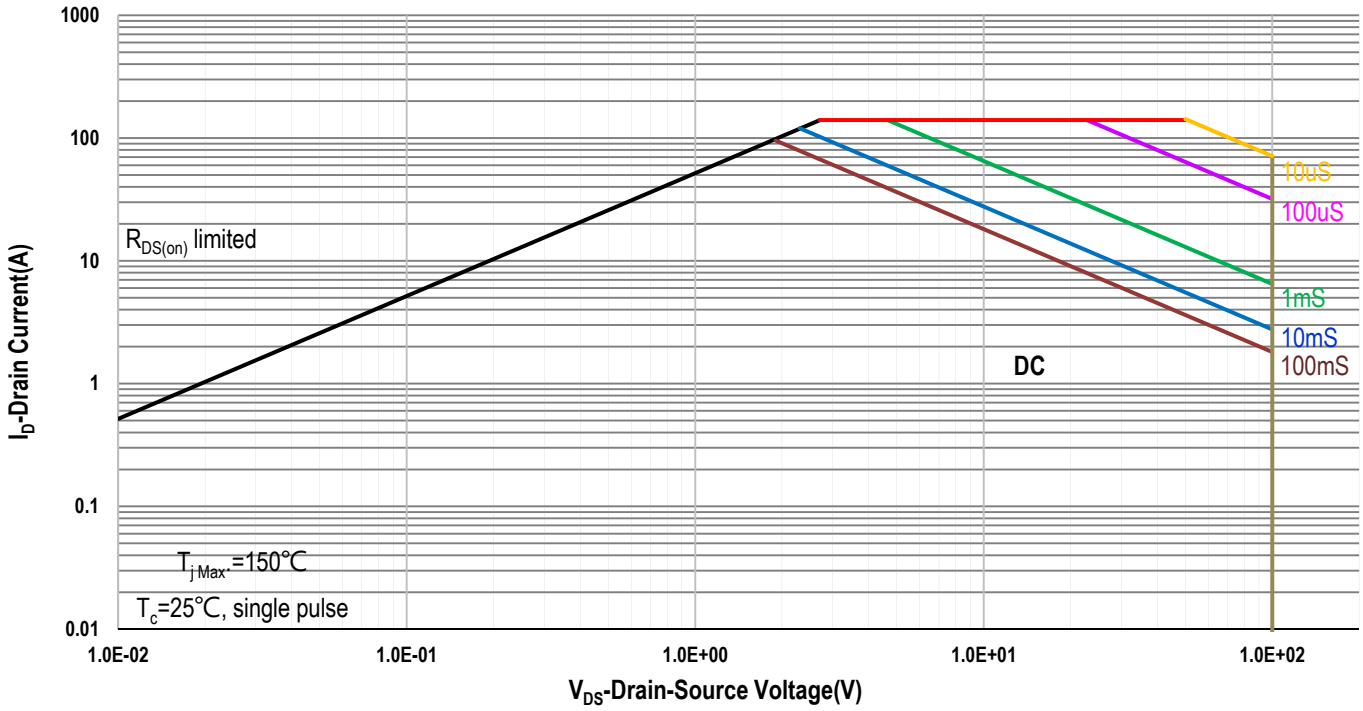
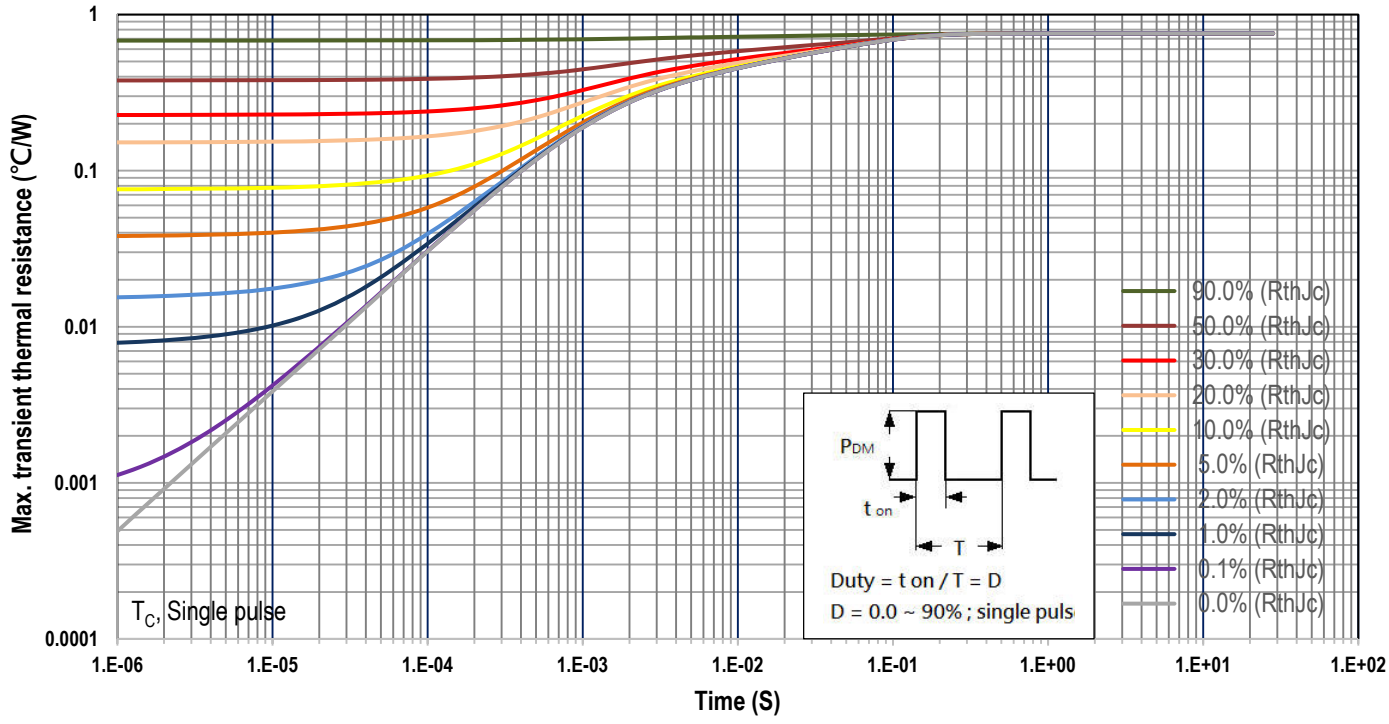
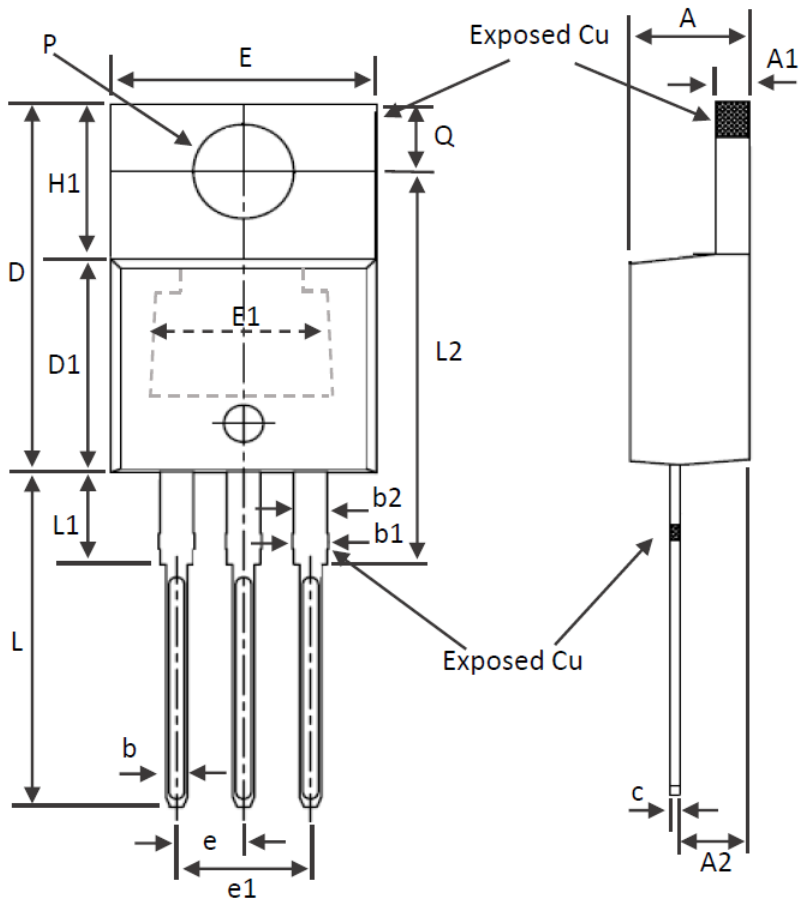


Fig. 14: Transient Thermal Impedance



Package of Dimension



Symbol	Min	Nor	Max
A	3.56	4.57	4.82
A1	0.51	1.27	1.39
A2	2.04	2.67	2.92
b	0.39	0.81	1.01
b1	1.15	1.37	1.82
b2	1.15	1.27	1.77
D	14.22	15.00	16.51
D1	8.39	8.70	9.01
D2	11.45	11.94	12.87
E	9.66	10.11	10.66
E1	6.86	7.00	8.89
e	2.54 Ref.		
e1	5.08 Ref.		
H1	5.85	6.30	6.85
L	12.70	13.60	14.73
L1	-	3.75	6.35
L2	15.80	16.00	16.20
P	3.54	3.87	4.08
Q	2.54	2.74	3.42

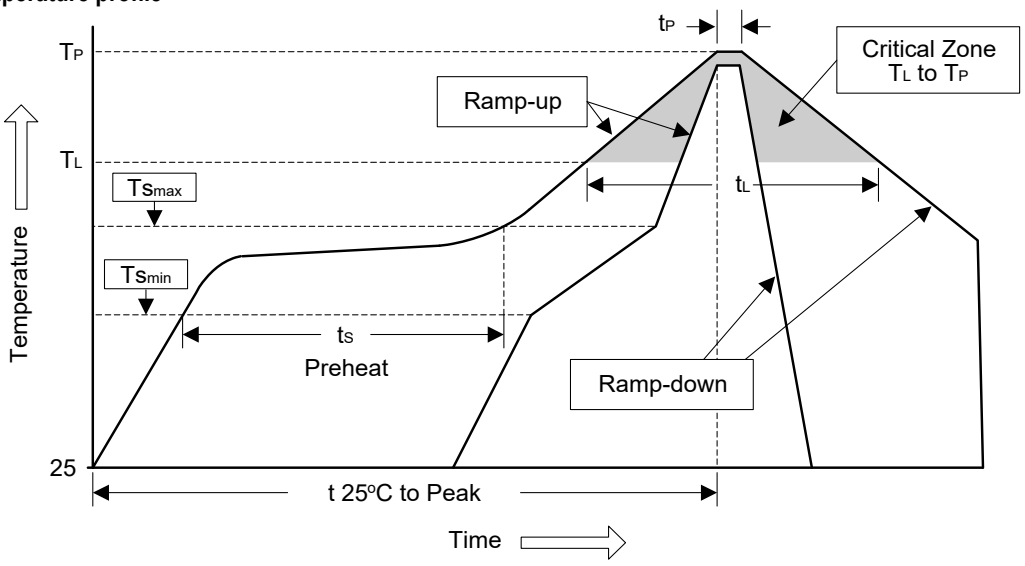
1. All dimension are in millimeters.
2. Dimension does not include burrs and mold flash/protrusions.

Appendix-A

Soldering Methods for Silicongear's Products (Just for SMD type of device)

1. Storage environment: Temperature=10°C to 35°C Humidity=65%±15%
2. Reflow soldering of surface-mount devices

Figure 1: Temperature profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (min to max) (ts)	 100°C 150°C 60 to 120 sec	 150°C 200°C 60 to 180 sec
Tsmax to T_L - Ramp-up Rate	 <3°C/sec	 <3°C/sec
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Peak Temperature (T_P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

Appendix-B

Important Notice

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