

Key parameter	N _{channel}	Unit
$V_{(BR)DSS}$ min.	-100	V
$R_{DS(ON)}$ max. $V_{GS}=-10V$	70.8	m Ω
$R_{DS(ON)}$ max. $V_{GS}=-4.5V$	79.2	m Ω
I_D	-15.1	A
$V_{GS(TH)}$ Typ.	-1.8	V
C_{iss} Typ.	3527	pF
Q_g 10V Typ.	60.5	nC

Package outline
PDFN 5x6-8L

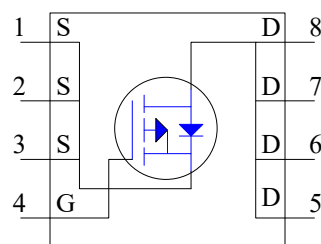
Description

The SG100P15Q used advanced trench technology of MOSFET to provide excellent electrical parameter. There is high speed switching capability, low $R_{DS(ON)}$ resistance, stabilizing qualified and characteristics for these devices. Moreover, it is had extreme high cell density in design. These features combine to be an advantage design for use in wide variety of application including small signal control and load switch application.

Features

- ◇ Fast switch capacity
- ◇ With voltage logic level driving characteristics
- ◇ Pb-free lead plating; RoHS compliant

Symbol and Pin assignment



Potential application

- Suitable for charging pile applications
- DC fan motor drive applications

Order Information

Item	Description
1. Order Code	SG100P15Q
2. Part Number	SG100P15Q
3. Package Type	PDFN5x6-8L
4. Package Code	Q
5. Packing Type	Tape & Reel
6. Quantity in Pack	2,500
7. RoHS Status	Halogen-Free

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1. Absolute Maximum Ratings ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous ^{Note 1}	$T_C=25^{\circ}\text{C}$	I_D	-15.1	A
	$T_C=100^{\circ}\text{C}$		-9.5	A
Drain Current-Continuous ^{Note 2}	$T_A=25^{\circ}\text{C}$	I_D	-2.8	A
	$T_A=70^{\circ}\text{C}$		-2.3	A
Drain Current-Pulsed ^{Note 3}	$T_A=25^{\circ}\text{C}$	I_{DM}	-70.0	A
Avalanche Current		I_{AR}	-14.5	A
Single Pulse Avalanche Energy ^{Note 4}		E_{AS}	10.5	mJ
Maximum Power Dissipation	$T_C=25^{\circ}\text{C}$	P_D	33.5	W
	$T_C=100^{\circ}\text{C}$		13.4	W
	$T_A=25^{\circ}\text{C}$		1.2	W
	$T_A=70^{\circ}\text{C}$		0.7	W
	Derate Factor Above $T_C=25^{\circ}\text{C}$		0.268	W/ $^{\circ}\text{C}$
Max. Operating Junction Temperature		T_J	150	$^{\circ}\text{C}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^{\circ}\text{C}$

2. Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal resistance, Junction-Case	$R_{\theta JC-P}$	Please refer to Note 5	-	-	3.7	$^{\circ}\text{C}/\text{W}$
Thermal resistance, Junction-Ambient	$R_{\theta JA-P}$	Please refer to Note 5	-	-	101	$^{\circ}\text{C}/\text{W}$

Notes:

- Limited by silicon chip capability and $R_{\theta JC-P}$ junction-to-case thermal resistance.
- The maximum current rating is limited by package and $R_{\theta JA-P}$ junction-to-ambient thermal resistance.
- Must be ensure junction temperature does not exceed 150-degree C. (Pulse Width $\leq 100\mu\text{s}$, Duty $\leq 2\%$)
- Limited by T_{Jmax} , starting $T_J=25^{\circ}\text{C}$, $L=0.1\text{mH}$, $R_g=25\Omega$, $I_D=-14.5\text{A}$, $V_{GS}=-10\text{V}$.
- The value of thermal resistance is measured with the single device mounted on 1 inch² FR-4 PCB with 2 oz. copper under a still air environment temperature is 25°C based on JEDEC standard JESD51-14 and JESD51-2a. Thermal resistance obtained depends on the user's specific board design and given application.

3. Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _{DS} =-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V	-	-	-1	μA
		V _{DS} =-100V, V _{GS} =0V, T _J =125°C	-	-	-100	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA

STATIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _{DS} =-250μA	-1.4	-1.8	-2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _{DS} =-5A	-	59.0	70.8	mΩ
		V _{GS} =-4.5V, I _{DS} =-3A	-	66.0	79.2	mΩ
Gate Resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	2	-	Ω
Forward Transconductance	g _{fs}	V _{DS} =-5V, I _{DS} =-5A	-	13.4	-	S

DYNAMIC CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C _{iss}	V _{DD} =-100V, V _{DS} =-50V, V _{GS} =0V, f=1MHz	-	3527	-	pF
Output Capacitance	C _{oss}	V _{DD} =-100V, V _{DS} =-50V, V _{GS} =0V, f=1MHz	-	107.4	-	pF
Reverse Transfer Capacitance	C _{rss}	V _{DD} =-100V, V _{DS} =-50V, V _{GS} =0V, f=1MHz	-	58.0	-	pF
Turn-On Delay Time	T _{d(on)}	V _{DS} =-50V, V _{GS} =-10V, I _{DS} =-5A, R _{GEN} =3Ω	-	15.0	-	nS
Rise Time	T _r	V _{DS} =-50V, V _{GS} =-10V, I _{DS} =-5A, R _{GEN} =3Ω	-	13.3	-	nS
Turn-Off Delay Time	T _{d(off)}	V _{DS} =-50V, V _{GS} =-10V, I _{DS} =-5A, R _{GEN} =3Ω	-	109.7	-	nS
Fall Time	T _f	V _{DS} =-50V, V _{GS} =-10V, I _{DS} =-5A, R _{GEN} =3Ω	-	35.7	-	nS

GATE CHARGE CHARACTERISTICS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Gate to Source Gate Charge	Q _{gs}	V _{DD} =-50V, I _D =-5A, V _{GS} =0 to -10V	-	13.0	-	nC
Gate charge at threshold	Q _{g(th)}	V _{DD} =-50V, I _D =-5A, V _{GS} =0 to -10V	-	7.0	-	nC
Gate to Drain Charge	Q _{gd}	V _{DD} =-50V, I _D =-5A, V _{GS} =0 to -10V	-	8.5	-	nC
Switching charge	Q _{SW}	V _{DD} =-50V, I _D =-5A, V _{GS} =0 to -10V	-	14.5	-	nC
Gate charge total	Q _{g 10V}	V _{DD} =-50V, I _D =-5A, V _{GS} =0 to -10V	-	60.5	-	nC
Gate charge total	Q _{g 4.5V}	V _{DD} =-50V, I _D =-5A, V _{GS} =0 to -4.5V	-	27.8	-	nC
Gate plateau voltage	V _{plateau}	V _{DD} =-50V, I _D =-5A, V _{GS} =0 to -10V	-	3.3	-	V
Gate charge total, sync. FET (Q _g - Q _{gd})	Q _{g(sync)}	V _{DS} =0.1V, V _{GS} =0 to -10V	-	51.9	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Body Diode continuous forward current	I _S	T _C =25°C	-	-	-14.9	A
Body Diode pulse current	I _{SM}	T _C =25°C	-	-	-70.0	A
Body Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-5A	-	-0.8	-1.2	V
Body Diode Reverse Recovery Time	t _{rr}	V _{DD} =-50V, I _F =-5A, di/dt=100A/μs	-	29.5	-	nS
		V _{DD} =-50V, I _F =-5A, di/dt=200A/μs	-	25.2	-	nC
Body Diode Reverse Recovery Charge	Q _{rr}	V _{DD} =-50V, I _F =-5A, di/dt=100A/μs	-	46.1	-	nS
		V _{DD} =-50V, I _F =-5A, di/dt=200A/μs	-	65.1	-	nC
Body Diode Reverse Recovery Current	I _{rm}	V _{DD} =-50V, I _F =-5A, di/dt=100A/μs	-	-3.6	-	A
		V _{DD} =-50V, I _F =-5A, di/dt=200A/μs	-	-6.3	-	A

4. Typical Operating Characteristics Diagram

Fig. 1: Output Characteristics

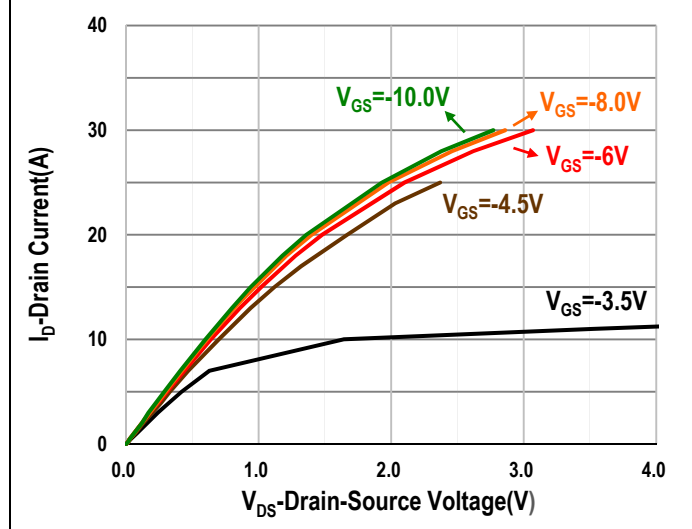


Fig. 2: Normalized $V_{(TH)GS}$ Voltage Vs. T_A

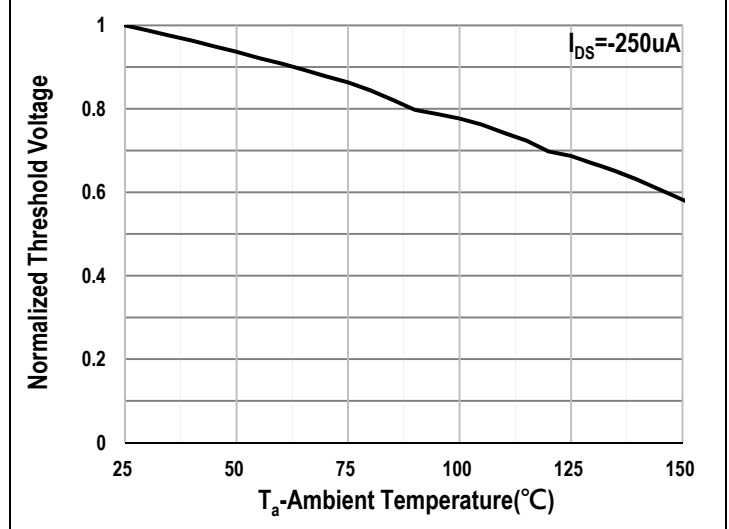


Fig. 3: Drain-Source On Resistance Vs V_{GS}

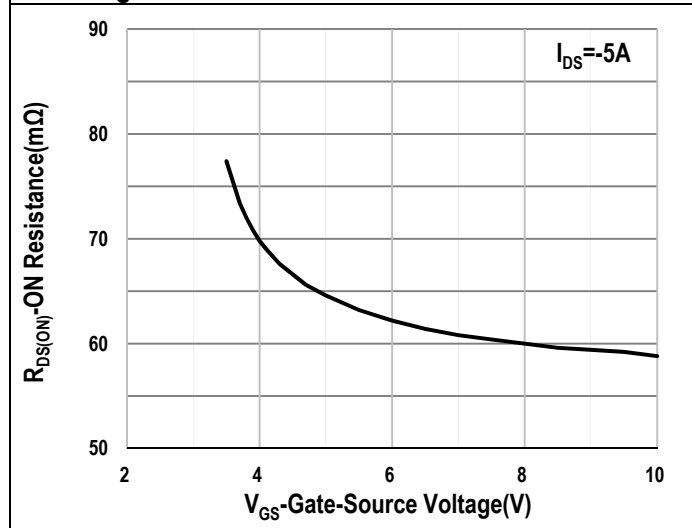


Fig. 4: Normalized $R_{DS(ON)}$ Resistance Vs. T_A

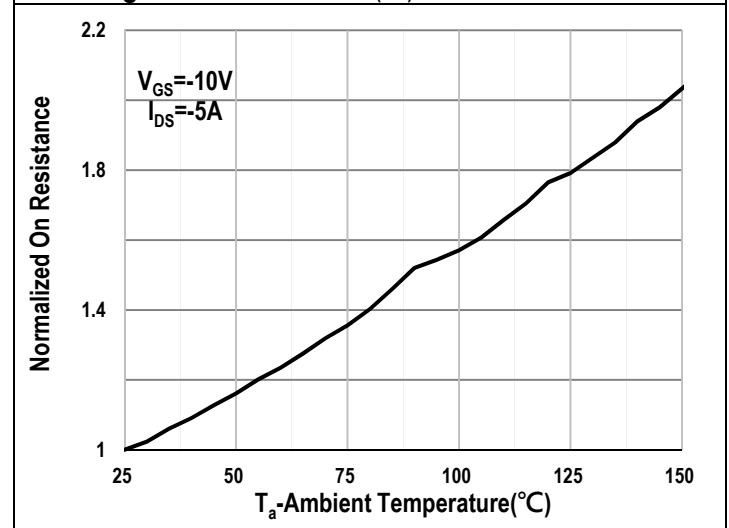


Fig. 5: Drain-Source On Resistance Vs I_D

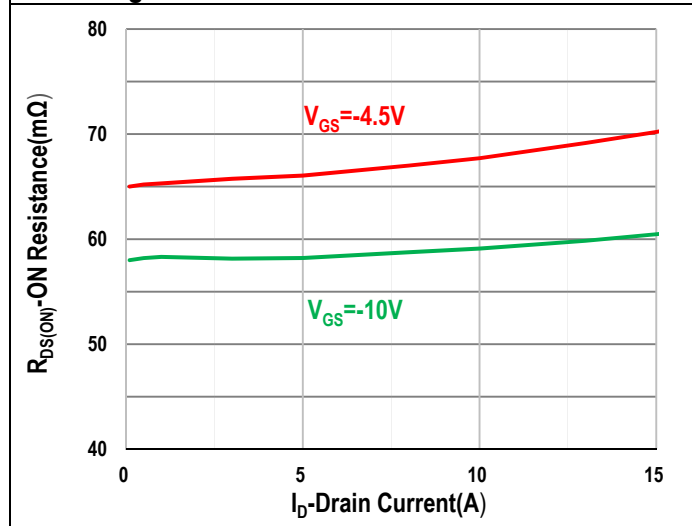
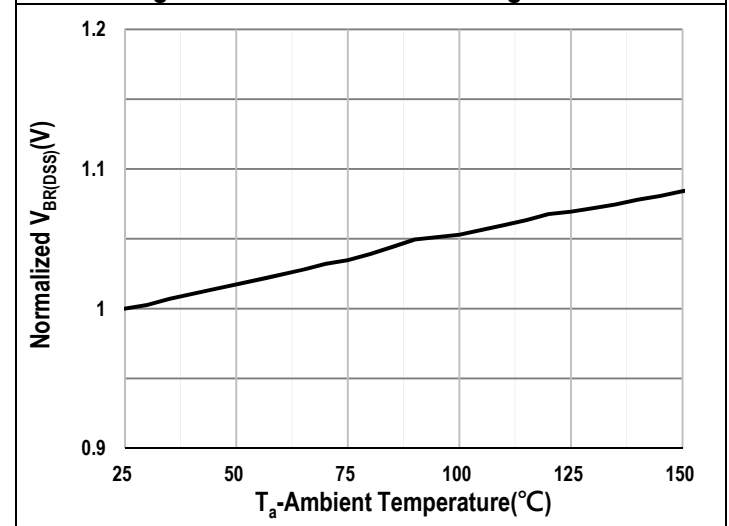


Fig. 6: Normalized BV_{DSS} Voltage Vs T_A



4. Typical Operating Characteristics Diagram

Fig. 7: Typical Capacitance Variation Vs V_{DS}

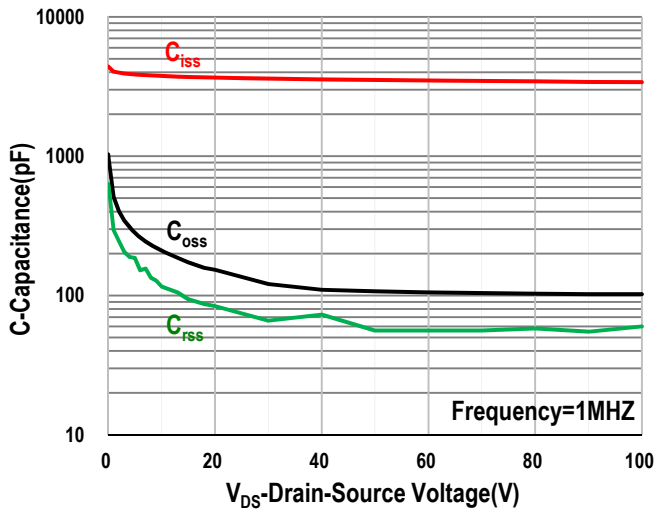


Fig. 8: Gate Charge Vs V_{GS}

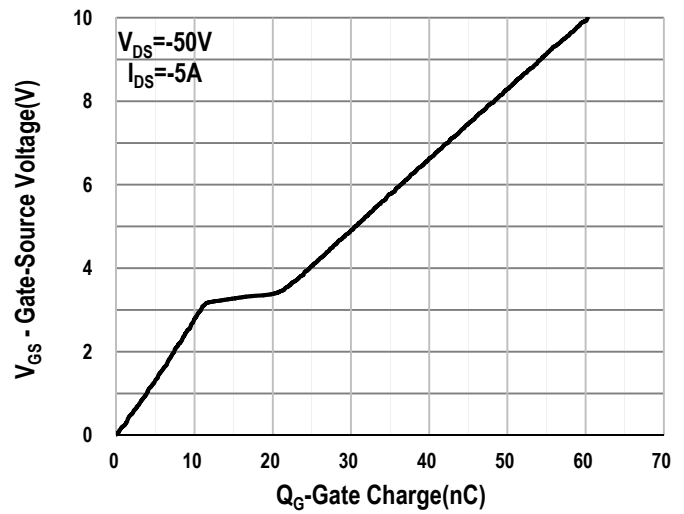


Fig. 9: Power Dissipation Vs. T_C

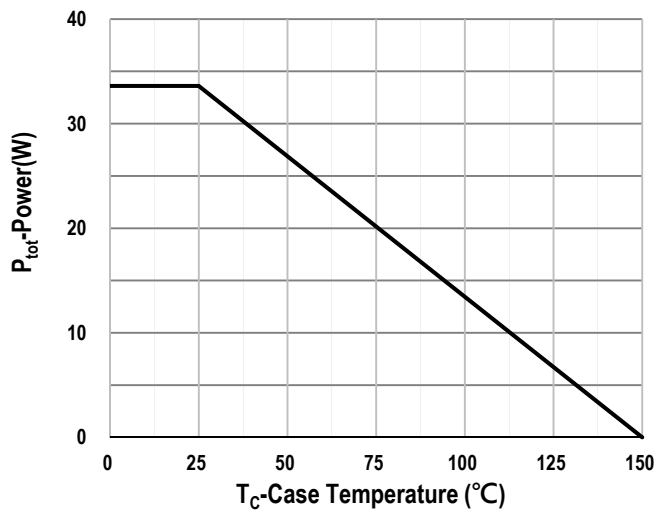


Fig. 10: Drain Current Vs. T_C

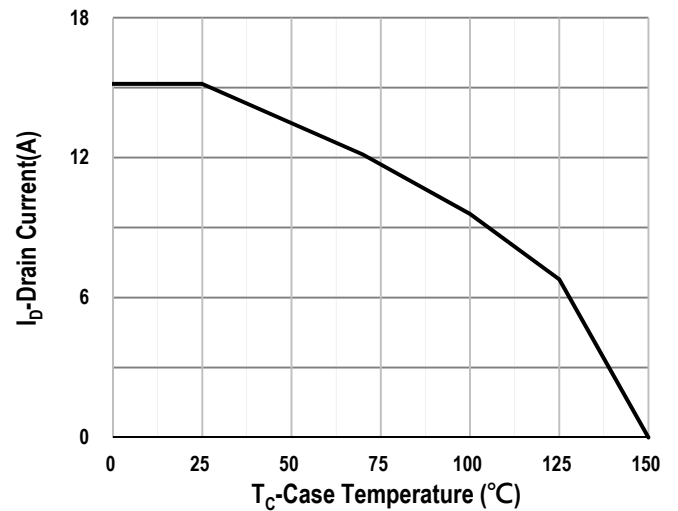


Fig. 11: Body Diode Forward Voltage Vs. I_S

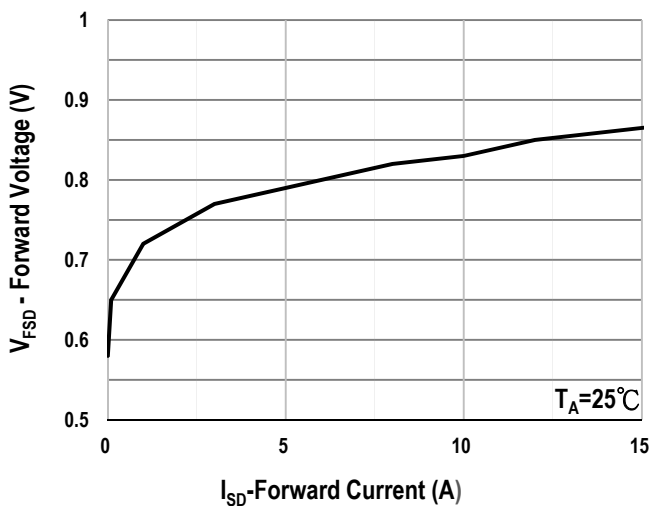
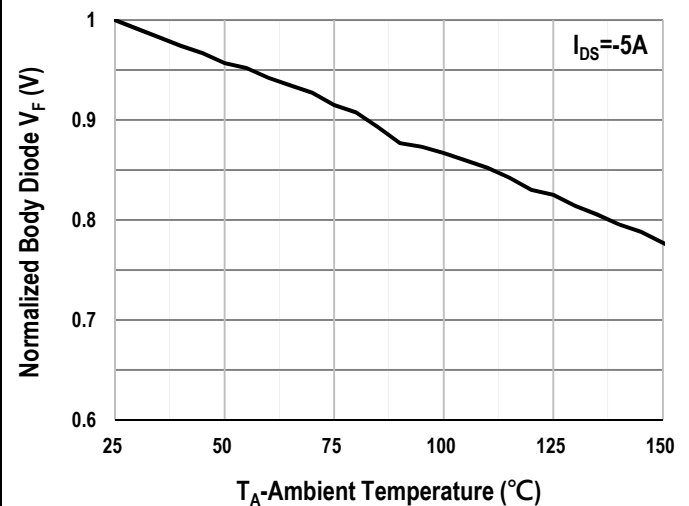


Fig. 12: Normalized Body Diode Forward Voltage Vs. T_A



4. Typical Operating Characteristics Diagram

Fig. 13: Safe Operation Area

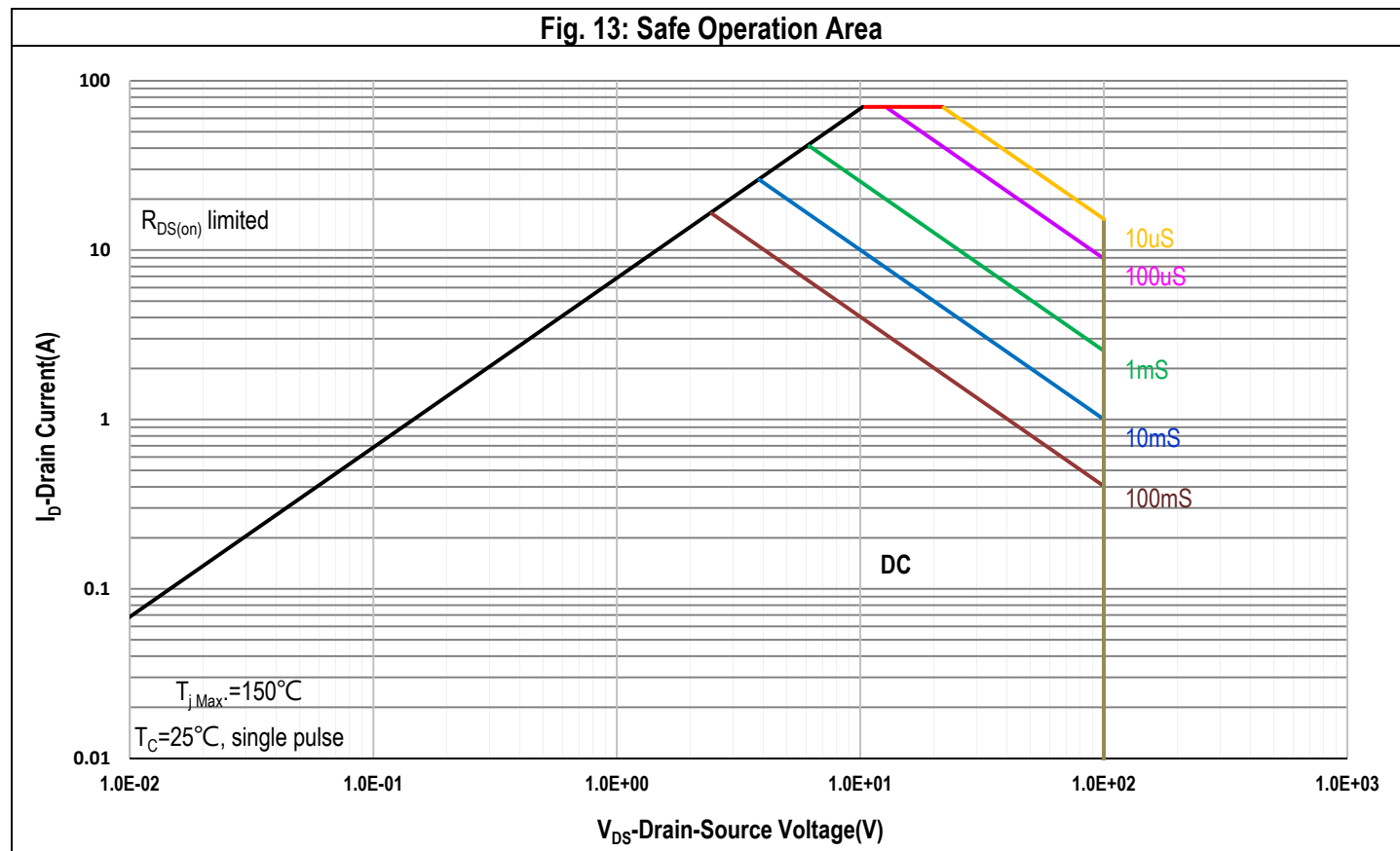
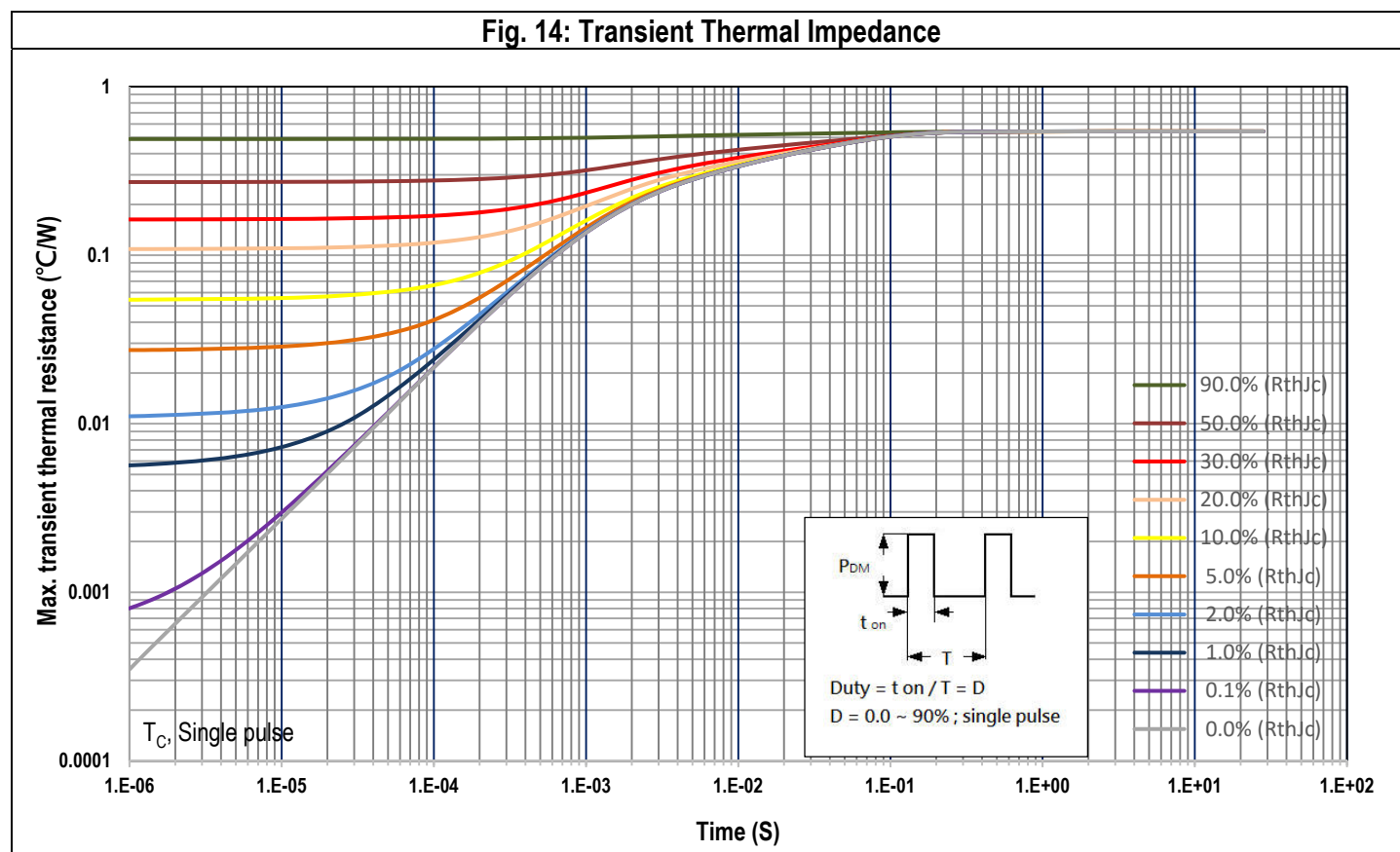
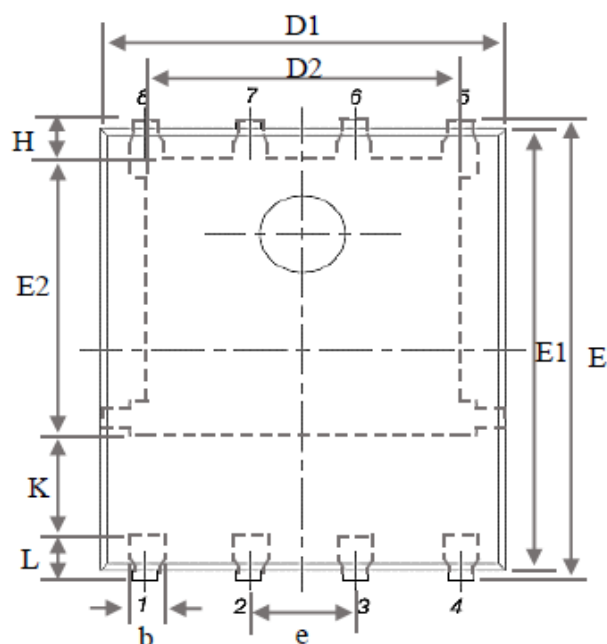


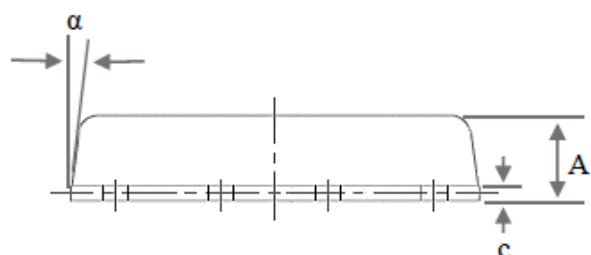
Fig. 14: Transient Thermal Impedance



5. Package of Dimension

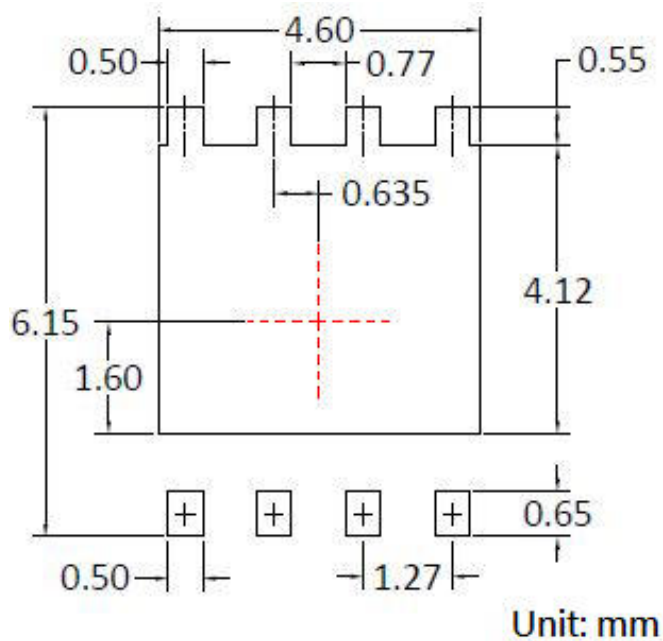


Symbol	Min	Nor	Max
A	0.90	1.04	1.17
b	0.33	0.42	0.51
C	0.06	0.20	0.35
D1	4.80	5.10	5.40
D2	3.61	3.96	4.31
E	5.90	6.03	6.15
E1	5.65	5.75	5.85
E2	3.30	3.54	3.78
e	1.27 BSC		
H	0.38	0.50	0.61
L	0.38	0.55	0.71
L1	0.05	0.15	0.25



1. All dimension are in millimeters.
2. Dimension does not include burrs and mold flash/protrusions.

6. Land pattern (Footprint)



Note 1: Land pattern (Footprint) design is for reference only.

Note 2: Package body sizes exclude mold flash and burrs.

Note 3: Dimension is measured in gauge plane.

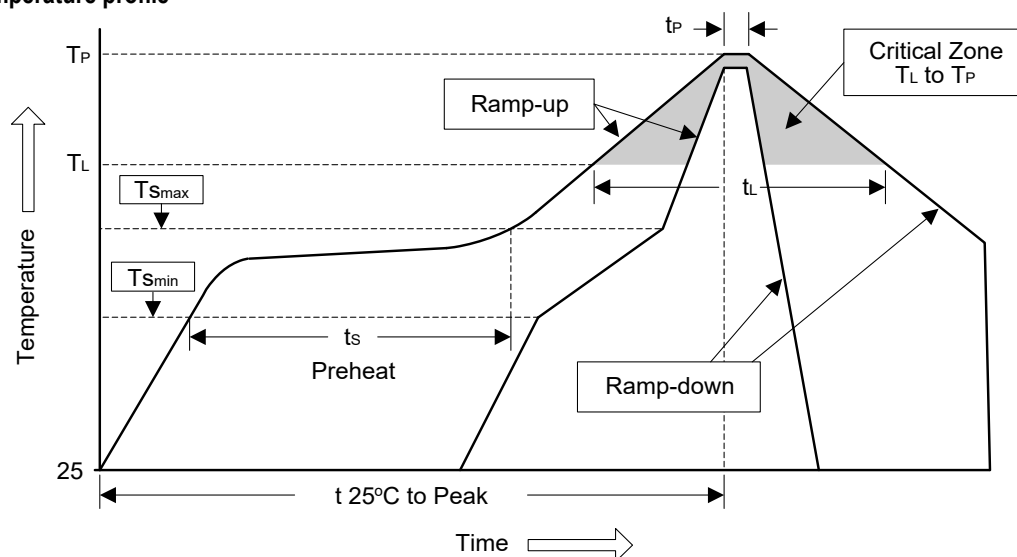
Note 4: Tolerance 0.1mm unless otherwise specified.

7. Appendix-A

Soldering Methods for Silicongear's Products (Just for SMD type of device)

- Storage environment: Temperature=10°C to 35°C Humidity=65%±15%
- Reflow soldering of surface-mount devices

Figure 1: Temperature profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TL to TP)	<3°C/sec	<3°C/sec
Preheat		
- Temperature Min (T _{min})	100°C	150°C
- Temperature Max (T _{max})	150°C	200°C
- Time (min to max) (ts)	60 to 120 sec	60 to 180 sec
T _{max} to TL		
- Ramp-up Rate	<3°C/sec	<3°C/sec
Time maintained above:		
- Temperature (TL)	183°C	217°C
- Time (tL)	60 to 150 sec	60 to 150 sec
Peak Temperature (TP)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

8. Appendix-B**Important Notice****© Silicongear Corporation**

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