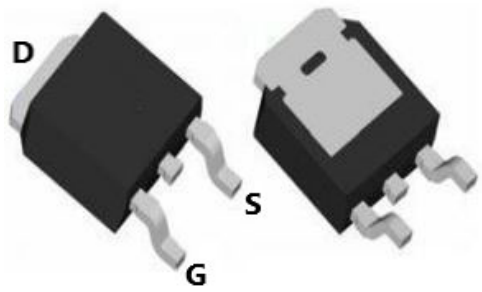
SG100P16D

100V P-Channel Enhanced Mode MOSFET

Key parameter	N channel	Unit
$V_{(BR)DSS\ min.}$	-100	V
$R_{DS\ (ON)\ max.}$ V_{GS}=-10V	206	mΩ
$R_{DS(ON)\ max.}$ V_{GS}=-4.5V	230	mΩ
I_D	-10.9	A
$V_{GS(TH)\ Typ.}$	-1.8	V
$C_{iss\ Typ.}$	1343	pF
$Q_{g\ 10V\ Typ.}$	23.8	nC

Package outline

TO-252



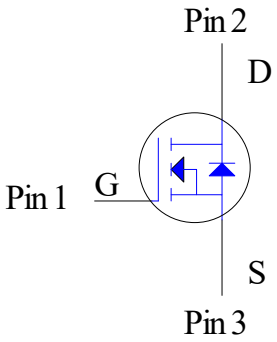
Description

The SG100P16D used advanced trench technology of MOSFET to provide excellent electrical parameter. There is high speed switching capability, low R_{DSON} resistance, stabilizing qualitied and characteristics for these devices. Moreover, it is had extreme high cell density in design. These features combine to be an advantage design for use in wide variety of application including small signal control and load switch application.

Features

- ◇ Fast switch capacity
- ◇ With voltage logic level driving characteristics
- ◇ Pb-free lead plating; RoHS compliant

Symbol and Pin assignment



Potential application

- ◯ Suitable for charging pile applications
- ◯ DC fan motor drive applications

Order Information

Item	Description
1. Order Code	SG100P16D
2. Part Number	SG100P16D
3. Package Type	TO-252
4. Package Code	D
5. Packing Type	Tape & Reel
6. Quantity in Pack	2,500
7. RoHS Status	Halogen-Free

Content

1. Absolute Maximum Ratings (T_J=25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	-100	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous Note 1	T_C=25°C	I_D	-10.9	A
	T_C=100°C		-6.9	A
Drain Current-Continuous Note 2	T_A=25°C	I_D	-2.0	A
	T_A=70°C		-1.6	A
Drain Current-Pulsed Note 3	T_A=25°C	I_{DM}	-33	A
Avalanche Current		I_{AR}	-4.8	A
Single Pulse Avalanche Energy Note 4		E_{AS}	1.1	mJ
Maximum Power Dissipation	T_C=25°C	P_D	48.4	W
	T_C=100°C		19.4	W
	T_A=25°C		1.6	W
	T_A=70°C		1.1	W
	Derate Factor Above T_C=25°C		0.38	W/°C
Max. Operating Junction Temperature		T_J	150	°C
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

2. Thermal Resistance Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Thermal resistance, Junction-Case	$R_{\Theta JC\text{-}P}$	Please refer to Note 5	-	-	2.5	°C/W
Thermal resistance, Junction-Ambient	$R_{\Theta JA\text{-}P}$	Please refer to Note 5	-	-	74.6	°C/W

Notes:

1. Limited by silicon chip capability and $R_{\Theta JC\text{-}P}$ junction-to-case thermal resistance.
2. The maximum current rating is limited by package and $R_{\Theta JA\text{-}P}$ junction-to-ambient thermal resistance.
3. Must be ensure junction temperature does not exceed 150-degree C. (Pulse Width≦100uS, Duty≦2%)
4. Limited by T_{Jmax}, starting T_J=25°C, L=0.1mH, R_g=25Ω, I_D=-4.8A, V_{GS}=-10V.
5. The value of thermal resistance is measured with the single device mounted on 1 inch^2 FR-4 PCB with 2 oz. copper under a still air environment temperature is 25℃ based on JEDEC standard JESD51-14 and JESD51-2a. Thermal resistance obtained depends on the user's specific board design and given application.

3. Electrical Characteristics (T_J=25°C unless otherwise noted)

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_{DS}=-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V, V_{GS}=0V	-	-	-1	μA
		V_{DS}=-100V, V_{GS}=0V, T_J=125°C	-	-	-100	μA
Gate-Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA

STATIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_{DS}=-250μA	-1.3	-1.8	-2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_{DS}=-3A	-	172	206	mΩ
		V_{GS}=-4.5V, I_{DS}=-2A	-	192	230	mΩ
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	-	13	-	Ω
Forward Transconductance	g_{fs}	V_{DS}=-5V, I_{DS}=-3A	-	7.1	-	S

DYNAMIC CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Capacitance	C_{iss}	V_{DD}=-100V, V_{DS}=-50V, V_{GS}=0V, f=1MHz	-	1343	-	pF
Output Capacitance	C_{oss}	V_{DD}=-100V, V_{DS}=-50V, V_{GS}=0V, f=1MHz	-	37.6	-	pF
Reverse Transfer Capacitance	C_{rss}	V_{DD}=-100V, V_{DS}=-50V, V_{GS}=0V, f=1MHz	-	30.2	-	pF
Turn-On Delay Time	$T_{d(on)}$	V_{DS}=-50V, V_{GS}=-10V, I_{DS}=-3A, R_{GEN}=10Ω	-	7.2	-	nS
Rise Time	T_r	V_{DS}=-50V, V_{GS}=-10V, I_{DS}=-3A, R_{GEN}=10Ω	-	9.5	-	nS
Turn-Off Delay Time	$T_{d(off)}$	V_{DS}=-50V, V_{GS}=-10V, I_{DS}=-3A, R_{GEN}=10Ω	-	77.6	-	nS
Fall Time	T_f	V_{DS}=-50V, V_{GS}=-10V, I_{DS}=-3A, R_{GEN}=10Ω	-	29.3	-	nS

GATE CHARGE CHARACTERISTICS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Gate to Source Gate Charge	Q_{gs}	V_{DD}=-50V, I_D=-3A, V_{GS}=0 to -10V	-	5.3	-	nC
Gate charge at threshold	$Q_{g(th)}$	V_{DD}=-50V, I_D=-3A, V_{GS}=0 to -10V	-	2.6	-	nC
Gate to Drain Charge	Q_{gd}	V_{DD}=-50V, I_D=-3A, V_{GS}=0 to -10V	-	3.3	-	nC
Switching charge	Q_{SW}	V_{DD}=-50V, I_D=-3A, V_{GS}=0 to -10V	-	6	-	nC
Gate charge total	$Q_{g\ 10V}$	V_{DD}=-50V, I_D=-3A, V_{GS}=0 to -10V	-	23.8	-	nC
Gate charge total	$Q_{g\ 4.5V}$	V_{DD}=-50V, I_D=-3A, V_{GS}=0 to -4.5V	-	10.8	-	nC
Gate plateau voltage	$V_{plateau}$	V_{DD}=-50V, I_D=-3A, V_{GS}=0 to -10V	-	3.4	-	V
Gate charge total, sync. FET (Q_g- Q_{gd})	$Q_{g(sync)}$	V_{DS}=0.1V, V_{GS}=0 to -10V	-	20.5	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Body Diode continuous forward current	I_S	T_C=25°C	-	-	-10.9	A
Body Diode pulse current	I_{SM}	T_C=25°C	-	-	-33	A
Body Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=-3A	-	-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	V_{DD}=-50V, I_F=-3A, di/dt=100A/μs	-	19.9	-	nS
		V_{DD}=-50V, I_F=-3A, di/dt=200A/μs	-	19	-	nC
Body Diode Reverse Recovery Charge	Q_{rr}	V_{DD}=-50V, I_F=-3A, di/dt=100A/μs	-	20.8	-	nS
		V_{DD}=-50V, I_F=-3A, di/dt=200A/μs	-	30.9	-	nC
Body Diode Reverse Recovery Current	I_{rm}	V_{DD}=-50V, I_F=-3A, di/dt=100A/μs	-	-2.7	-	A
		V_{DD}=-50V, I_F=-3A, di/dt=200A/μs	-	-4.3	-	A

4. Typical Operating Characteristics Diagram

Fig. 1: Output Characteristics

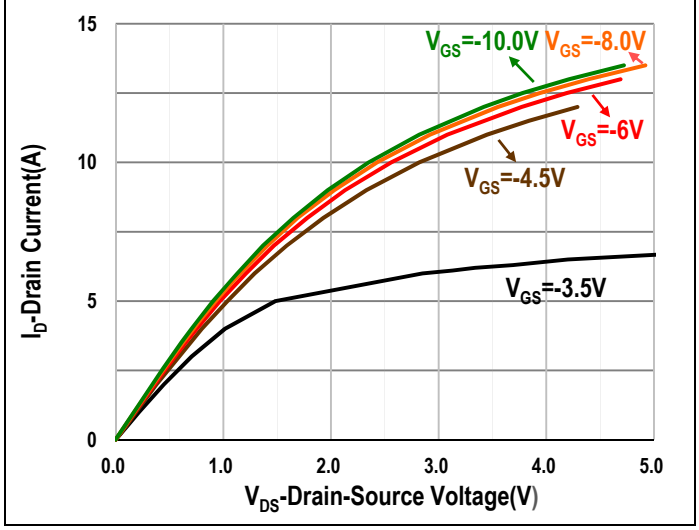


Fig. 2: Normalized $V_{(TH)GS}$ Voltage Vs. T_A

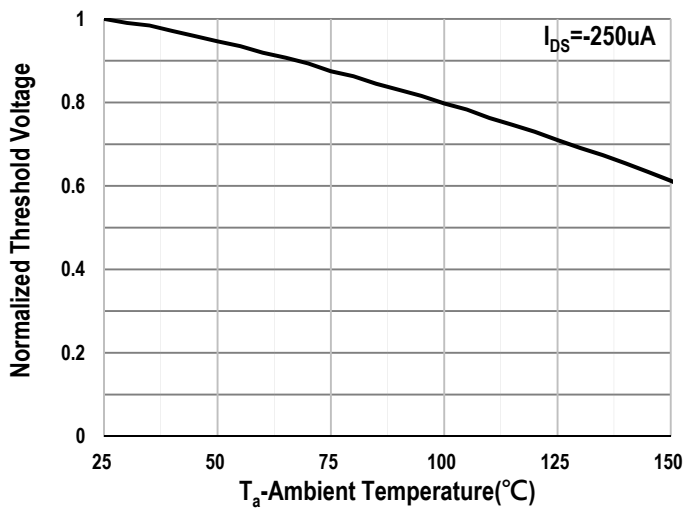


Fig. 3: Drain-Source On Resistance Vs V_{GS}

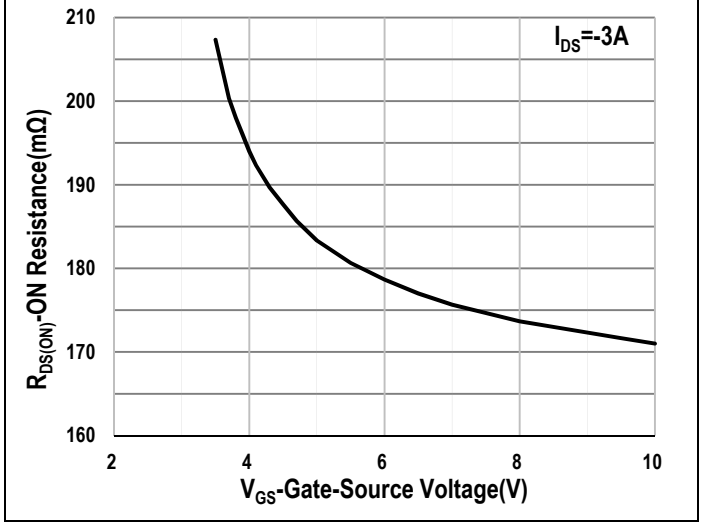


Fig. 4: Normalized $R_{DS(ON)}$ Resistance Vs. T_A

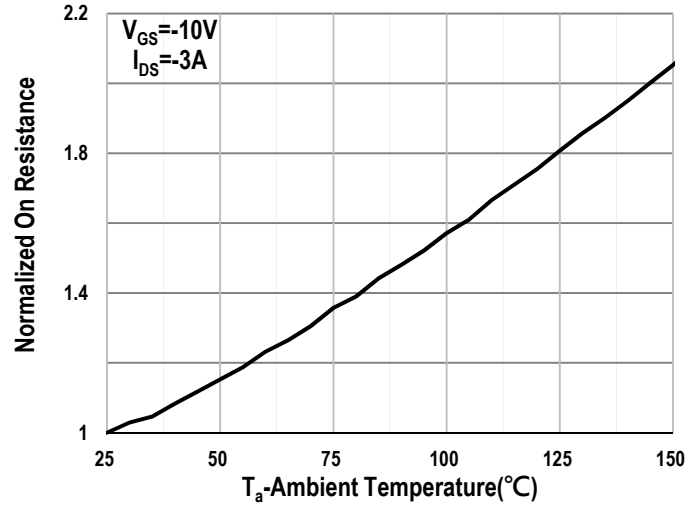


Fig. 5: Drain-Source On Resistance Vs I_D

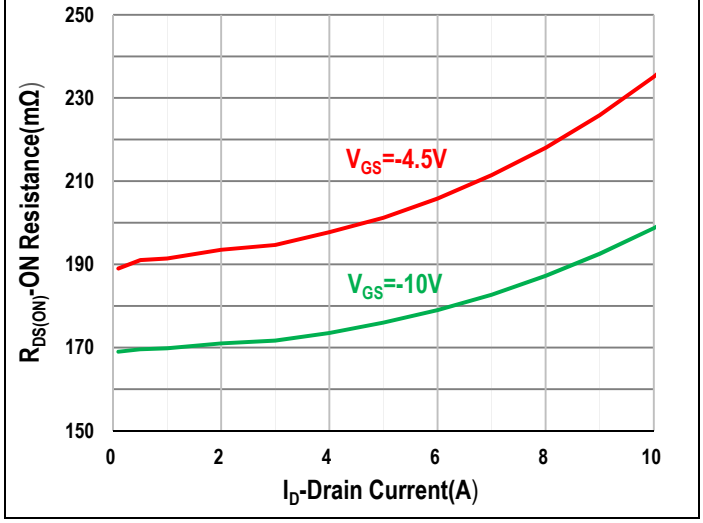
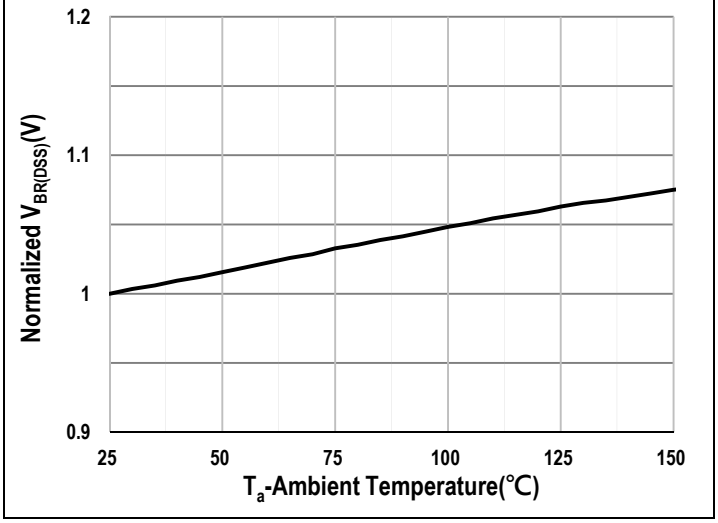


Fig. 6: Normalized BV_{DSS} Voltage Vs T_A



4. Typical Operating Characteristics Diagram

Fig. 7: Typical Capacitance Variation Vs V_{DS}

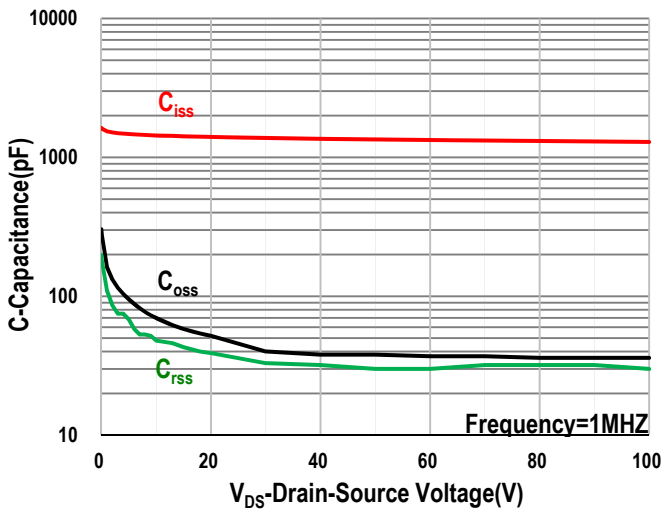


Fig. 8: Gate Charge Vs V_{GS}

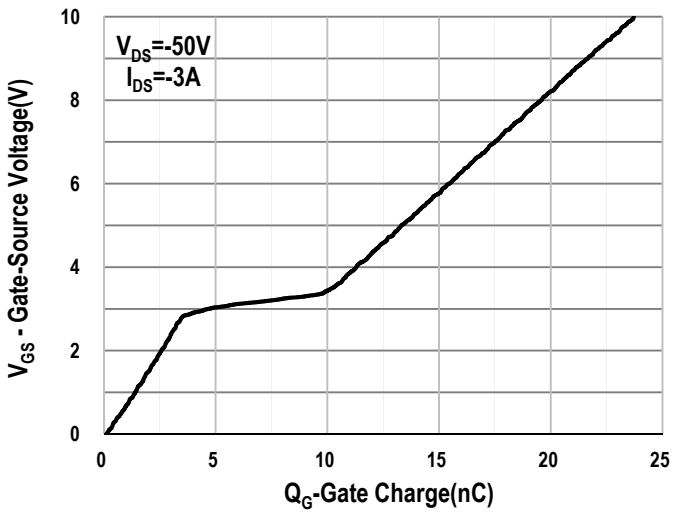


Fig. 9: Power Dissipation Vs. T_C

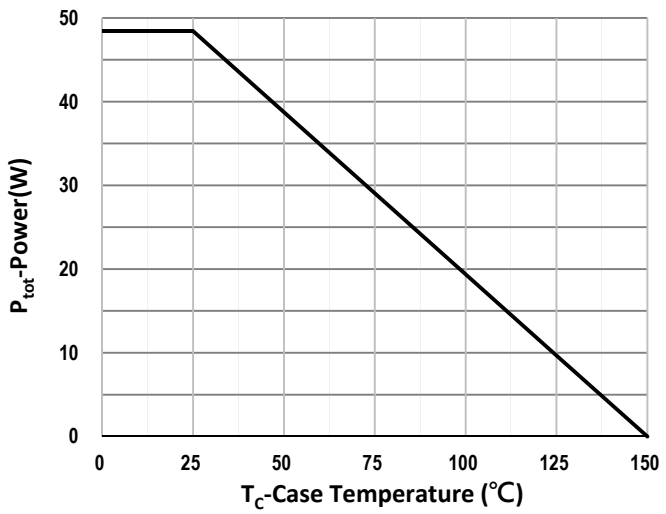


Fig. 10: Drain Current Vs. T_C

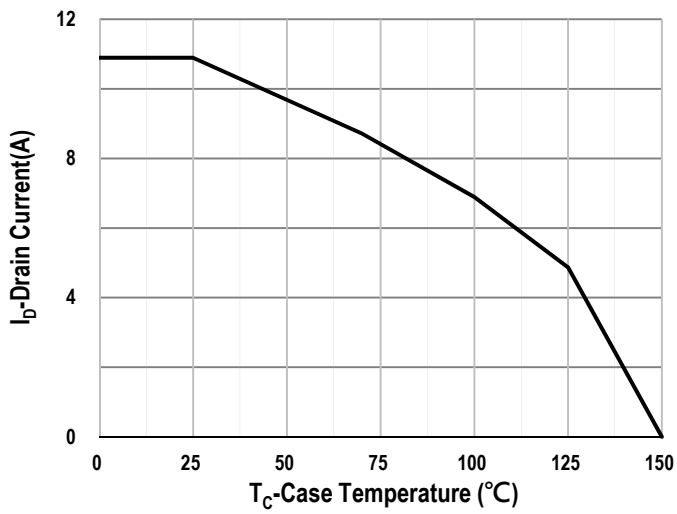


Fig. 11: Body Diode Forward Voltage Vs. I_S

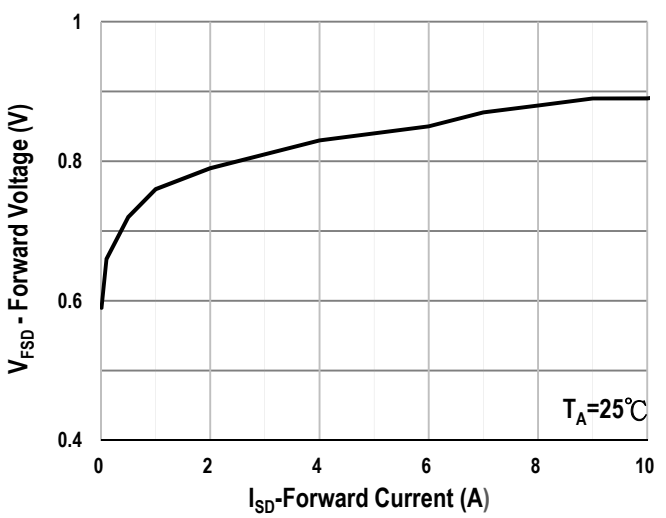
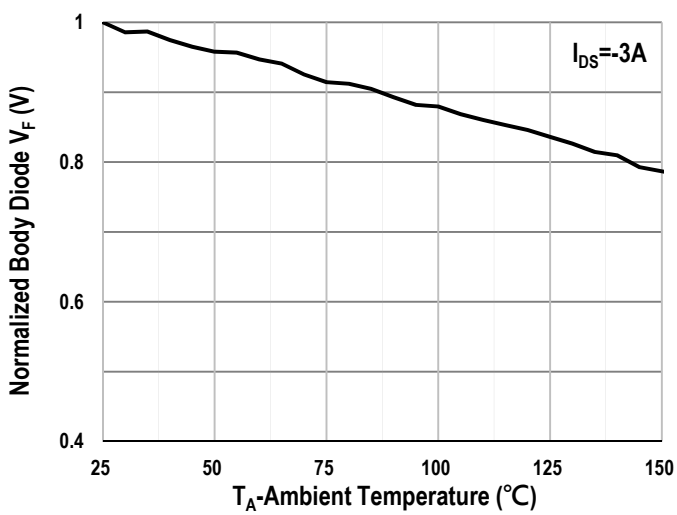


Fig. 12: Normalized Body Diode Forward Voltage Vs. T_A



4. Typical Operating Characteristics Diagram

Fig. 13: Safe Operation Area

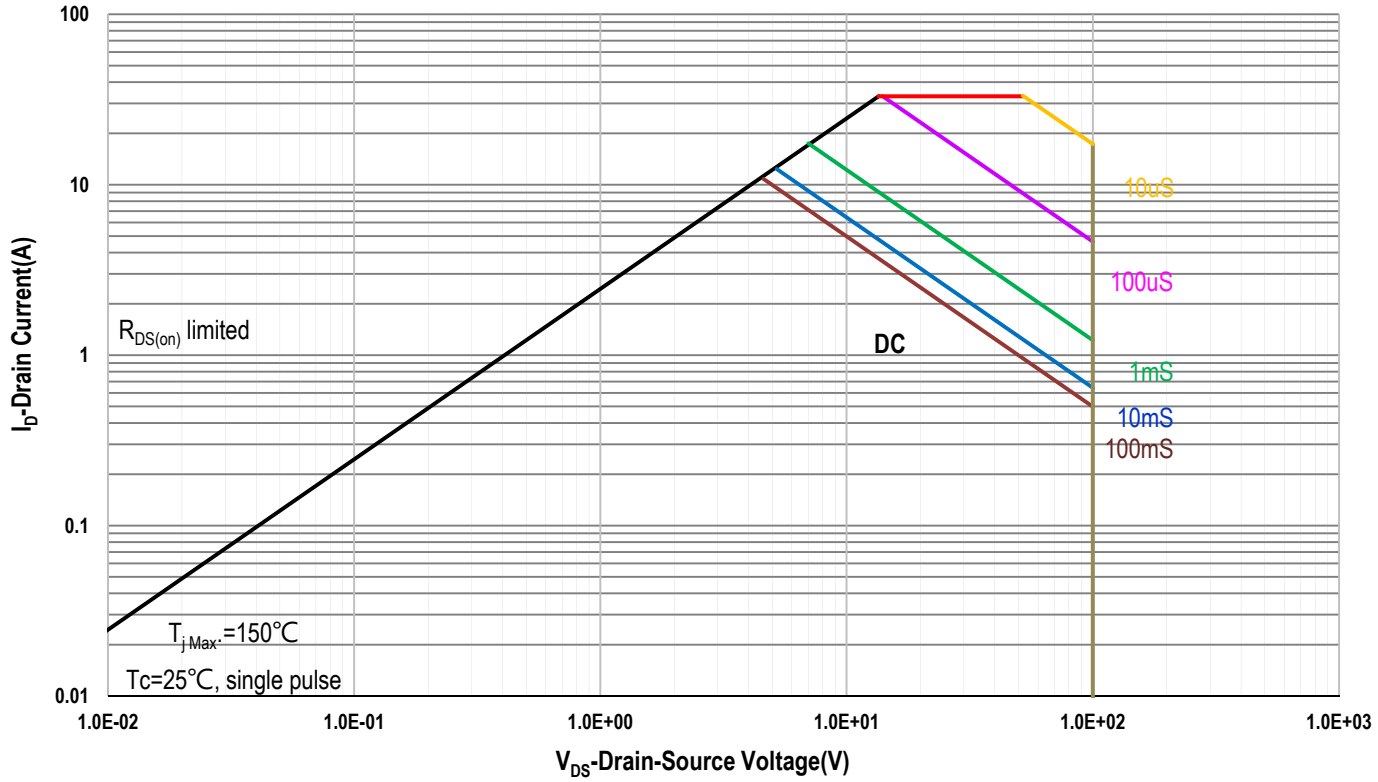
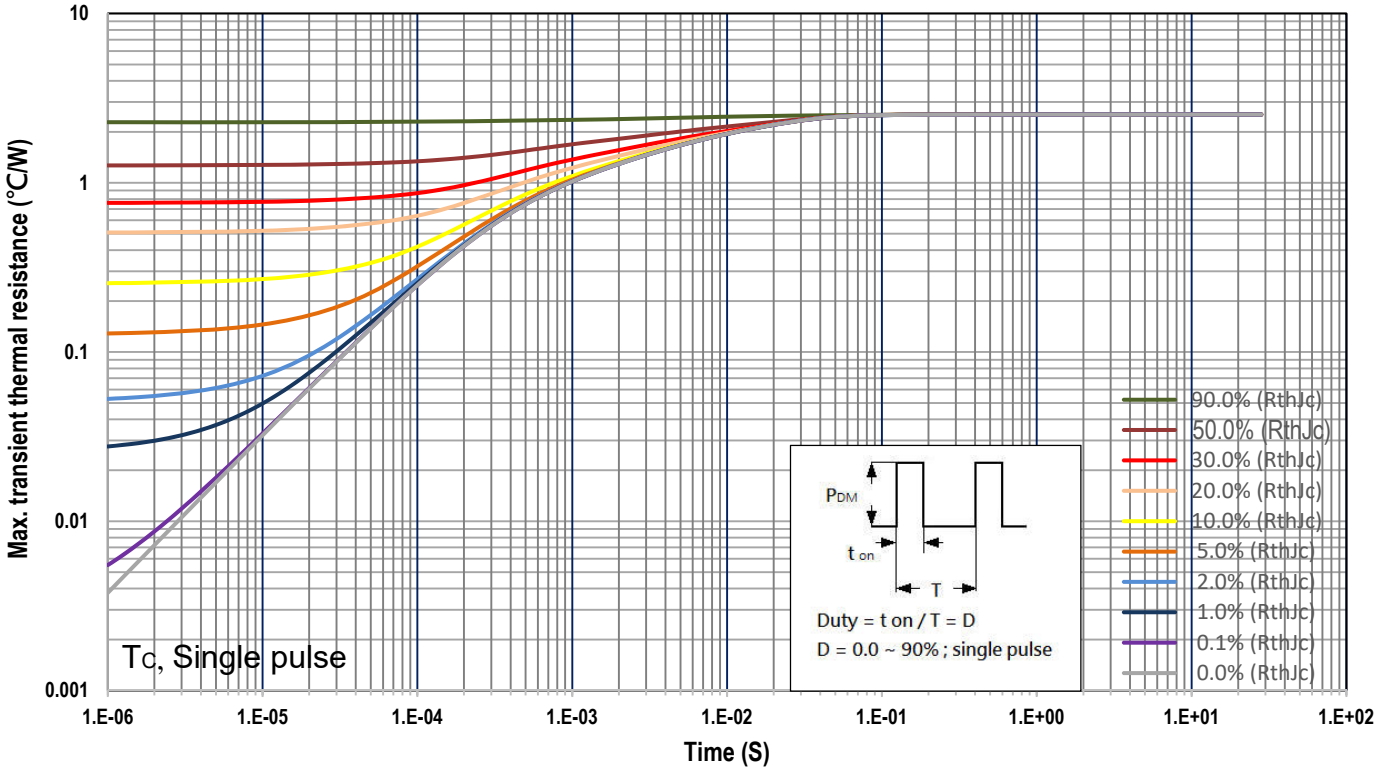
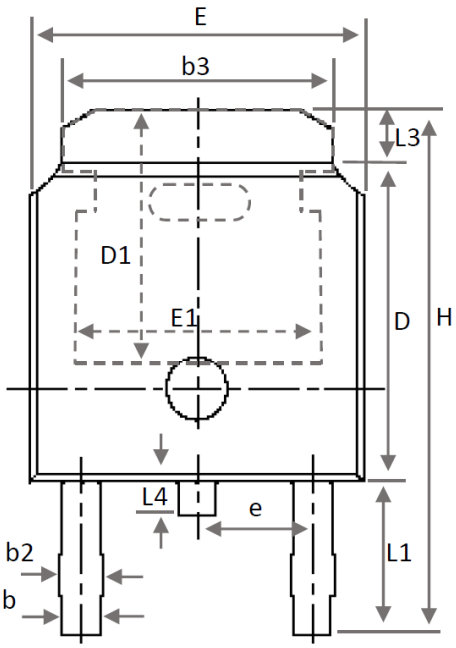
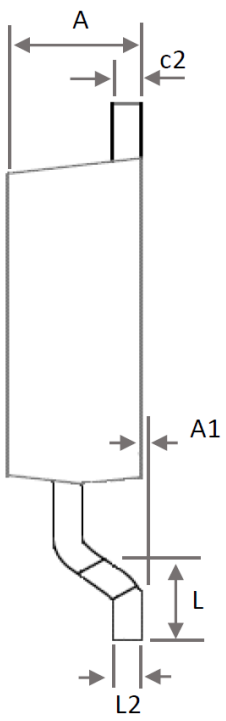


Fig. 14: Transient Thermal Impedance



5. Package of Dimension

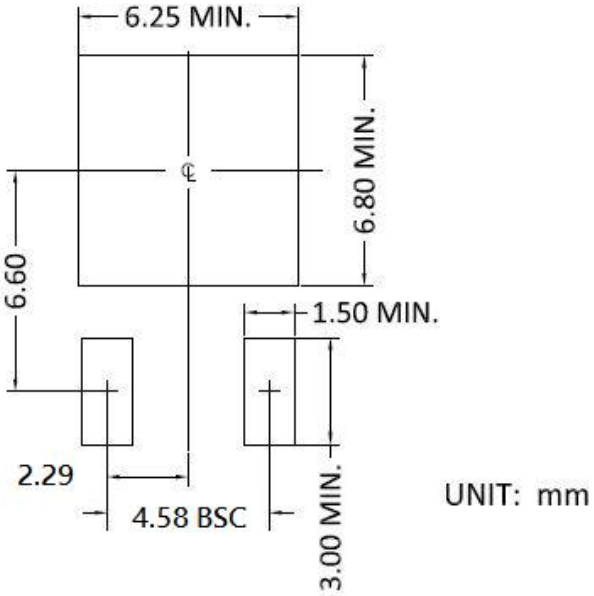




Symbol	Min	Nor	Max
E	6.35	6.54	6.731
L	1.40	1.59	1.78
L1		2.743 Ref.	
L2		0.508 BSC	
L3	0.89	1.08	1.27
L4	0.60	0.81	1.01
D	5.97	6.10	6.223
H	9.40	9.91	10.41
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	4.95	5.21	5.46
e		2.286 BSC	
A	2.18	2.29	2.39
A1	0.00	0.07	0.13
c2	0.46	0.68	0.89
D1	5.21	-	-
E1	4.32	-	-

1. All dimension are in millimeters.
2. Dimension does not include burrs and mold flash/protrusions.

6.Land pattern (Footprint)



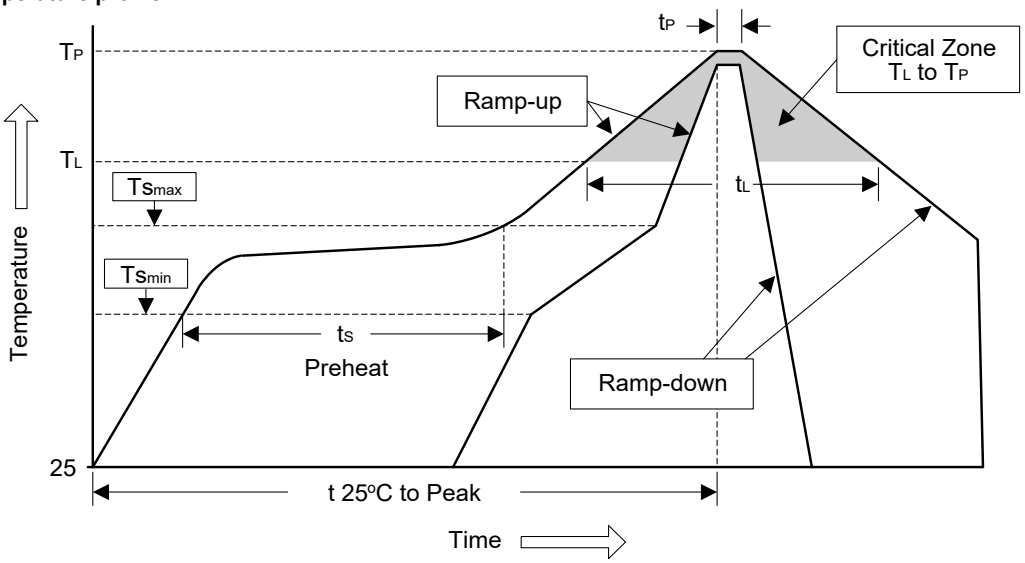
Note 1: Land pattern (Footprint) design is for reference only.
Note 2: Package body sizes exclude mold flash and burrs.
Note 3: Dimension is measured in gauge plane.
Note 4: Tolerance 0.1mm unless otherwise specified.

7. Appendix-A

Soldering Methods for Silicongear's Products (Just for SMD type of device)

1. Storage environment: Temperature=10°C to 35°C Humidity=65%±15%
2. Reflow soldering of surface-mount devices

Figure 1: Temperature profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	<3°C/sec	<3°C/sec
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (min to max) (ts)	 100°C 150°C 60 to 120 sec	 150°C 200°C 60 to 180 sec
Tsmax to T_L - Ramp-up Rate	 <3°C/sec	 <3°C/sec
Time maintained above: - Temperature (T_L) - Time (t_L)	 183°C 60 to 150 sec	 217°C 60 to 150 sec
Peak Temperature (T_P)	240°C +0/-5°C	260°C +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10 to 30 sec	20 to 40 sec
Ramp-down Rate	<6°C/sec	<6°C/sec
Time 25°C to Peak Temperature	<6 minutes	<8 minutes

3. Flow (wave) soldering (solder dipping)

Products	Peak Temperature	Dipping Time
Pb devices.	245°C ±5°C	5sec ±1sec
Pb-Free devices.	260°C +0/-5°C	5sec ±1sec

8. Appendix-B

Important Notice